

# N-Channel 60 V (D-S) MOSFET

## PRODUCT SUMMARY

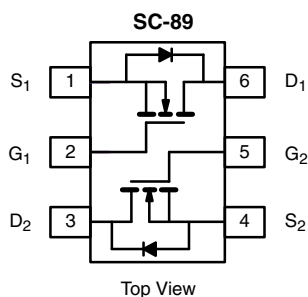
$V_{DS(min)}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$V_{GS(th)}$ (V)	$I_D$ (mA)
60	1.40 at $V_{GS} = 10$ V	1 to 2.5	500

## FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low On-Resistance: 1.40  $\Omega$
- Low Threshold: 2 V (typ.)
- Low Input Capacitance: 30 pF
- Fast Switching Speed: 15 ns (typ.)
- Low Input and Output Leakage
- ESD Protected: 2000 V
- Miniature Package
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



Marking Code: E

**Ordering Information:** Si1026X-T1-GE3 (Lead (Pb)-free and Halogen-free)

## BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Error Voltage
- Small Board Area

## APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	60		V
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	320	305	mA
		230	220	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	- 650		
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	450	380	
Maximum Power Dissipation <sup>a</sup>	$P_D$	280	250	mW
		145	130	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000		V

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

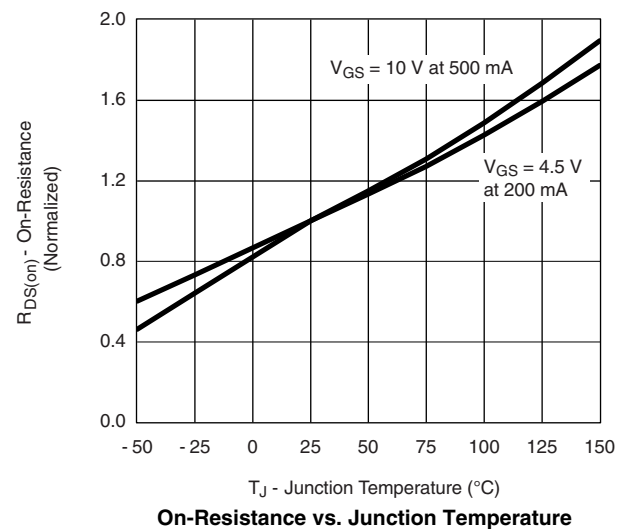
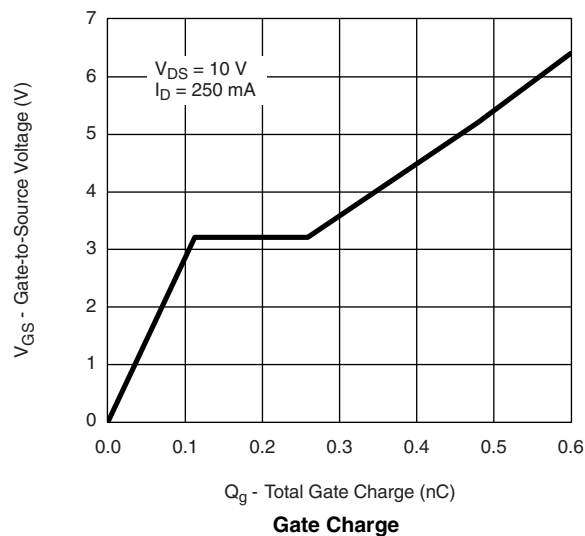
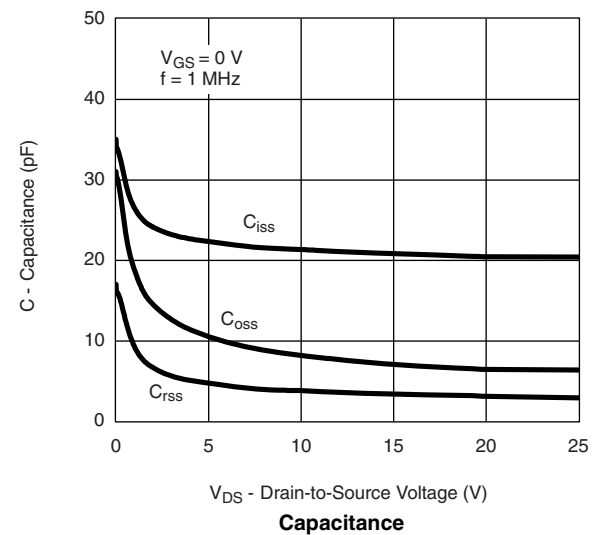
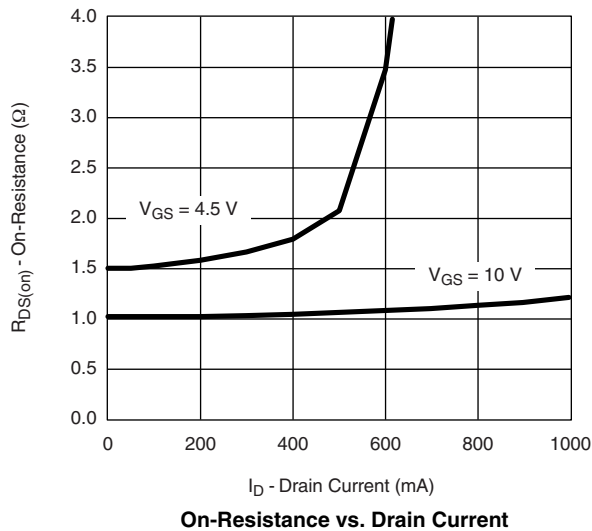
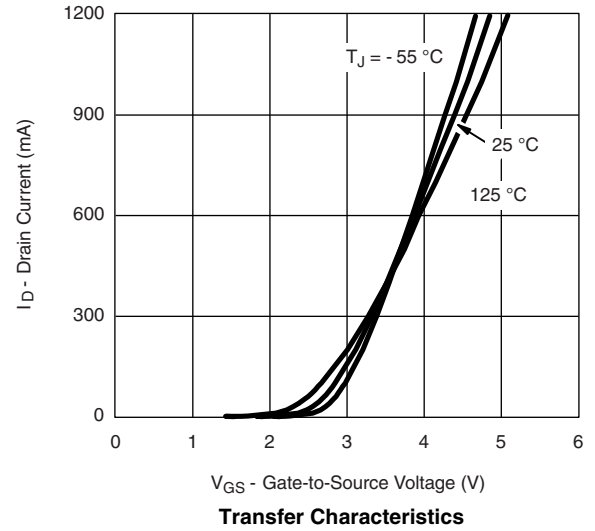
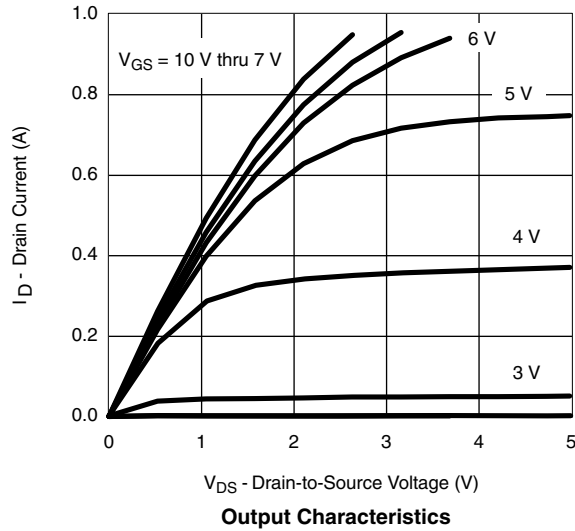
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 μA	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.25 mA	1		2.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 10 V			± 150	nA
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 5 V			± 50	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V	500			mA
		V <sub>DS</sub> = 7.5 V, V <sub>GS</sub> = 10 V	800			
Drain-Source On-Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 200 mA			3.0	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 500 mA			1.40	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 500 mA, T <sub>J</sub> = 125 °C			2.50	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 200 mA		200		mS
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 200 mA			1.40	V
Dynamic <sup>b</sup>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 250 mA, V <sub>GS</sub> = 4.5 V		600		pC
Gate-Source Charge	Q <sub>gs</sub>			120		
Gate-Drain Charge	Q <sub>gd</sub>			225		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		30		pF
Output Capacitance	C <sub>oss</sub>			6		
Reverse Transfer Capacitance	C <sub>rss</sub>			3		
Switching <sup>b, c</sup>						
Turn-On Time	t <sub>(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 150 Ω		15		ns
Turn-Off Time	t <sub>(off)</sub>	I <sub>D</sub> = 200 mA, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 10 Ω		20		

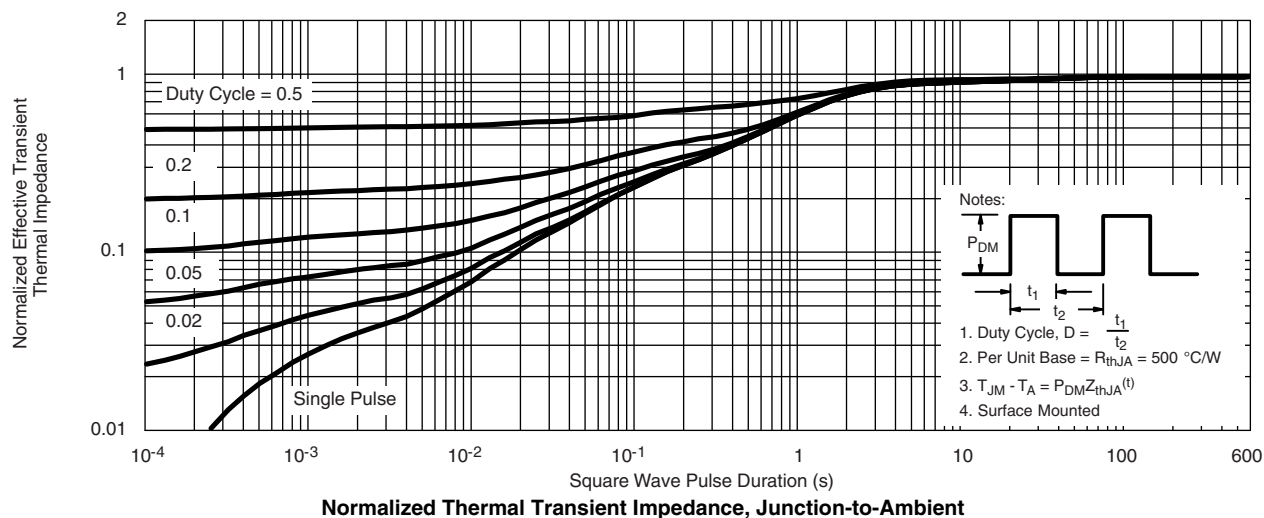
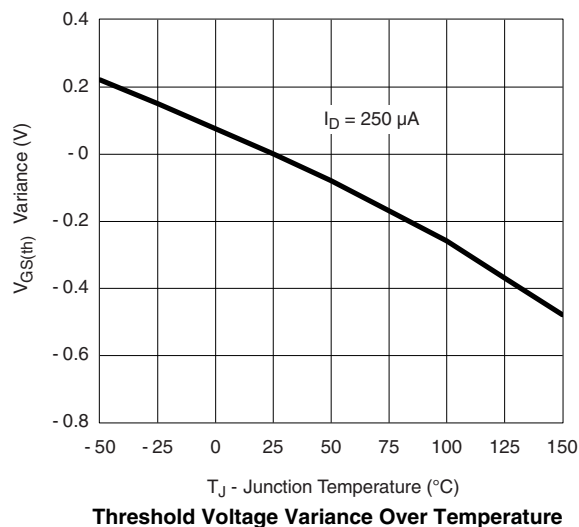
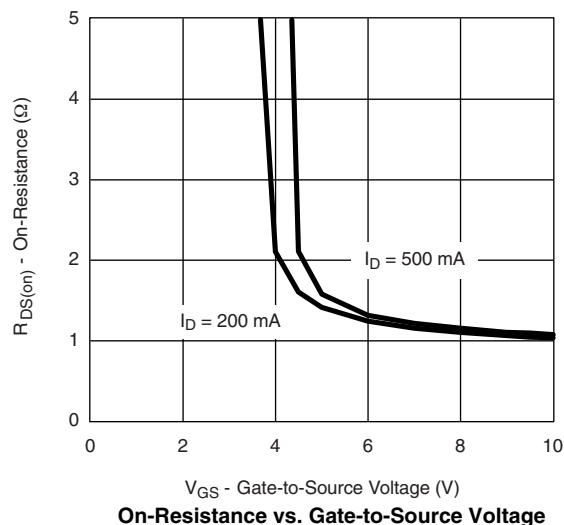
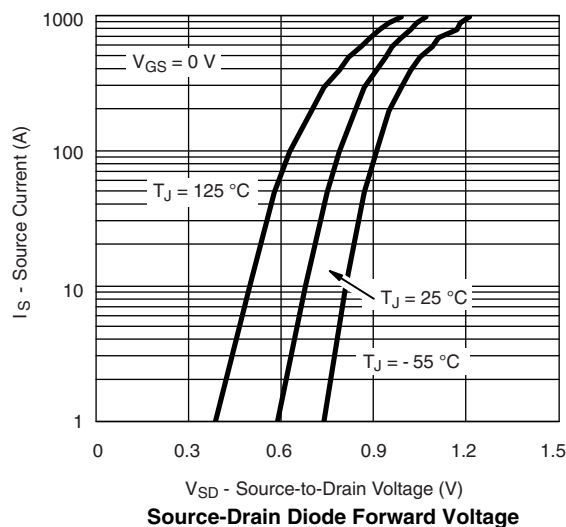
## Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. For DESIGN AID ONLY, not subject to production testing.  
c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

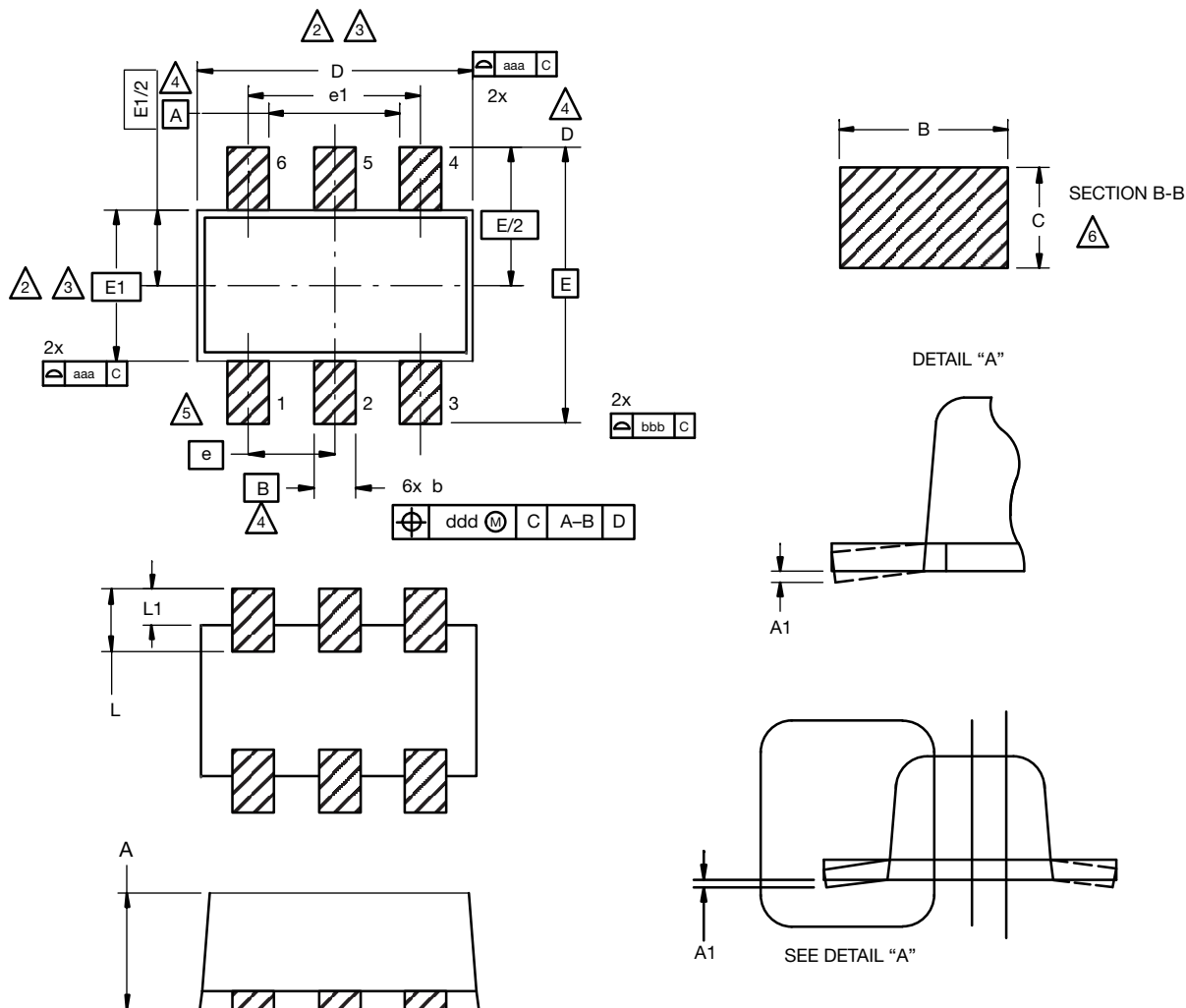
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg771434](http://www.vishay.com/ppg771434).

## SC-89 6-Leads (SOT-563F)



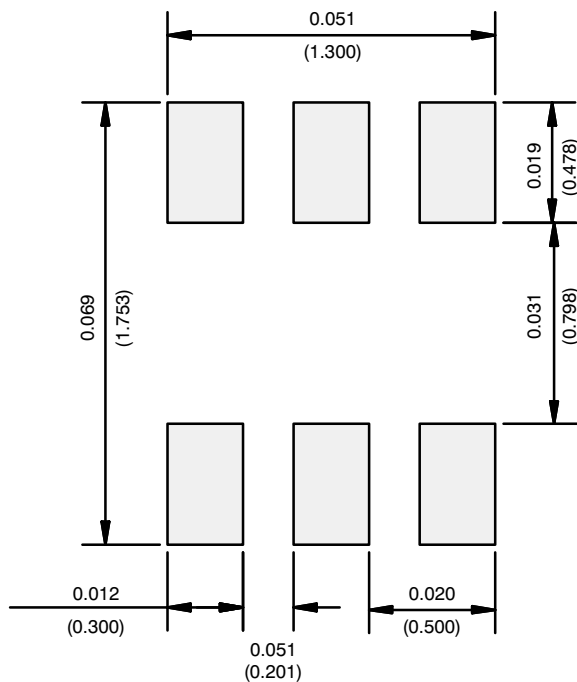
### Notes

1. Dimensions in millimeters.
- ⚠ Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- ⚠ Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- ⚠ Datums A, B and D to be determined 0.10 mm from the lead tip.
- ⚠ Terminal numbers are shown for reference only.
- ⚠ These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

C14-0439-Rev. C, 11-Aug-14  
DWG: 5880

## RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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