50 A VRPower® Integrated Power Stage
(Datasheet in Brief)

DESCRIPTION
The SiC657 is integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay’s proprietary 5 mm x 5 mm MLP package, SiC657 enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay’s state-of-the-art Gen IV TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC657 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V PWM logic.

A user selectable diode emulation mode (ZCD_EN#) is included to improve the light load performance. The device also supports PS4 mode to reduce power consumption when system operates in standby state.

FEATURES
• Thermally enhanced PowerPAK® MLP55-31L package
• Vishay’s Gen IV MOSFET technology and a low side MOSFET with integrated Schottky diode
• Delivers in excess of 50 A continuous current, 55 A at 10 ms peak current
• High efficiency performance
• High frequency operation up to 2 MHz
• Power MOSFETs optimized for 19 V input stage
• 5 V PWM logic with tri-state and hold-off
• Supports PS4 mode light load requirement for IMVP8 with low shutdown supply current (5 V, 3 μA)
• Under voltage lockout for VCIN

APPLICATIONS
• Multi-phase VRDs for computing, graphics card and memory
• Intel IMVP-8 VRPower delivery
- \( V_{\text{CORE}} \), \( V_{\text{GRAPHICS}} \), \( V_{\text{SYSTEM \ AGENT}} \) Skylake, Kabylake platforms
- \( V_{\text{CGI}} \) for Apollo Lake platforms
• Up to 24 V rail input DC/DC VR modules

TYPICAL APPLICATION DIAGRAM

Fig. 1 - Typical Application Diagram
### PRODUCT SUMMARY

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<th>Part number</th>
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<th>SiC657</th>
<th>SiC657A</th>
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<td>50 A power stage, 4.5 V\text{\textsubscript{IN}} to 24 V\text{\textsubscript{IN}}, 5 V PWM with ZCD, PS4 mode</td>
<td>50 A power stage, 4.5 V\text{\textsubscript{IN}} to 24 V\text{\textsubscript{IN}}, 3.3 V PWM with ZCD, PS4 mode</td>
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<td>Input voltage max. (V)</td>
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<td>Continuous current rating max. (A)</td>
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<tr>
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To request the full version of the datasheet, please contact: ICmarketing@vishay.com
# PowerPAK® MLP55-31L Case Outline

## Package Information

For technical questions, contact: powerictechsupport@vishay.com

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## DIM. | MILLIMETERS | INCHES
--- | --- | ---
A | 0.70 | 0.275
A1 | 0.00 | -
A2 | 0.20 | 0.008
b | 0.20 | 0.08
b1 | 0.15 | 0.006
D | 4.90 | 0.193
E | 4.90 | 0.193
L | 0.35 | 0.013
D2-1 | 0.98 | 0.039
D2-2 | 0.98 | 0.041
D2-3 | 1.87 | 0.074
D2-4 | 0.30 | 0.012
D2-5 | 1.05 | 0.041
E2-1 | 1.27 | 0.050
E2-2 | 1.93 | 0.078
E2-3 | 3.75 | 0.148
E2-4 | 0.45 | 0.018
F1 | 0.15 | 0.006
F2 | 0.20 | 0.008
F3 | 0.15 | 0.006

**MLP55-31L**

(5 mm x 5 mm)
## Notes

1. Use millimeters as the primary measurement.
3. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
4. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
5. Exact shape and size of this feature is optional.
6. Package warpage max. 0.08 mm.

### Table: DIMENSIONS

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<th>INCHES</th>
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For technical questions, contact: powerictechsupport@vishay.com

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Recommended Land Pattern
PowerPAK® MLP55-31L

Top side transparent view
(not bottom view)

Land pattern for MLP55-31L

All dimensions in millimeters

Component for MLP55-31L

Land pattern for MLP55-31L
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