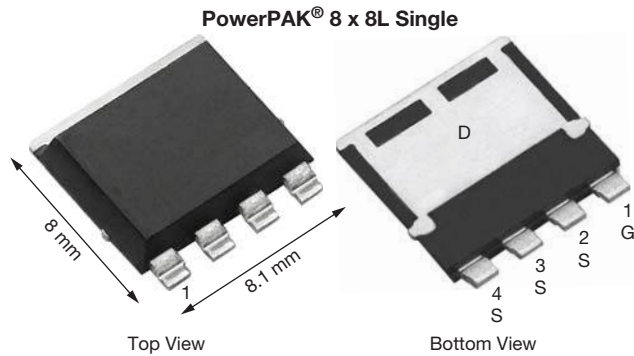
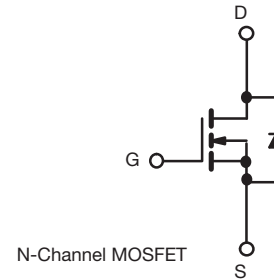


# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

**FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Thin 1.9 mm height
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0015
$I_D$ (A)	200
Configuration	Single
Package	PowerPAK 8 x 8L

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	40	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25$ °C <sup>a</sup>	200
		$T_C = 125$ °C	141
Continuous source current (diode conduction)	$I_S$	136	A
Pulsed drain current <sup>b</sup>	$I_{DM}$	600	
Single pulse avalanche current	$I_{AS}$	70	
Single pulse avalanche energy	$E_{AS}$	L = 0.1 mH	245
Maximum power dissipation			$P_D$
Operating junction and storage temperature range	$T_J, T_{stg}$	$T_C = 25$ °C	-55 to +175
		$T_C = 125$ °C	50
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	50	°C/W
Junction-to-case (drain)			

**Notes**

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.5	3	3.5	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	500	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	-	0.0011	0.0015	$\Omega$
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0021	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0025	
Forward transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		-	122	-	S
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	11 367	14 780	$\mu\text{F}$
Output capacitance	$C_{oss}$			-	6000	7800	
Reverse transfer capacitance	$C_{rss}$			-	615	800	
Total gate charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	-	125	165	nC
Gate-source charge <sup>c</sup>	$Q_{gs}$			-	35	-	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	13	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$		0.45	0.99	1.50	$\Omega$
Turn-on delay time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	22	32	ns
Rise time <sup>c</sup>	$t_r$			-	8	14	
Turn-off delay time <sup>c</sup>	$t_{d(off)}$			-	52	73	
Fall time <sup>c</sup>	$t_f$			-	14	20	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed current <sup>a</sup>	$I_{SM}$			-	-	200	A
Forward voltage	$V_{SD}$	$I_F = 50\text{ A}, V_{GS} = 0\text{ V}$		-	0.8	1.1	V

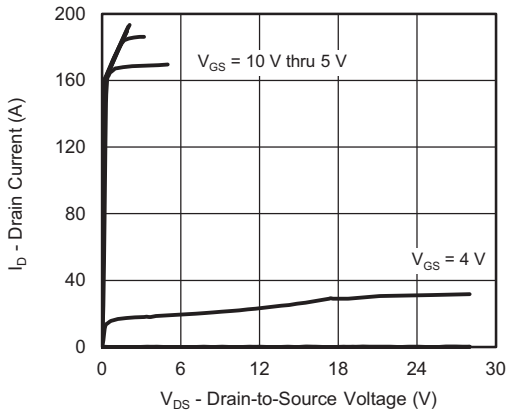
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

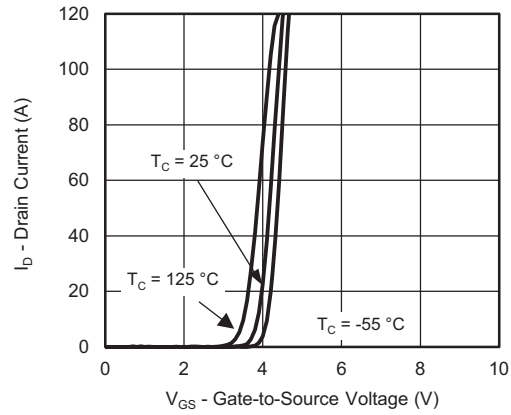
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



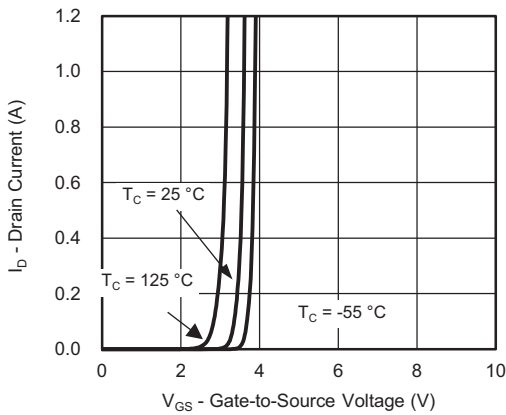
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



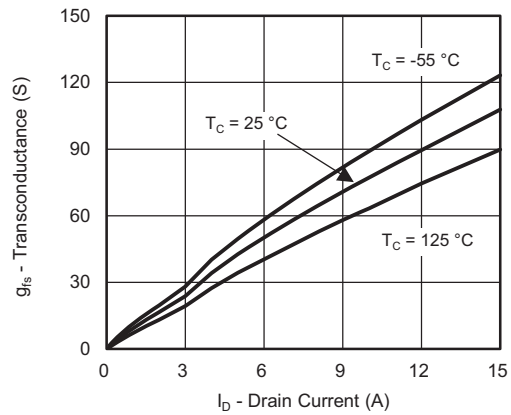
Output Characteristics



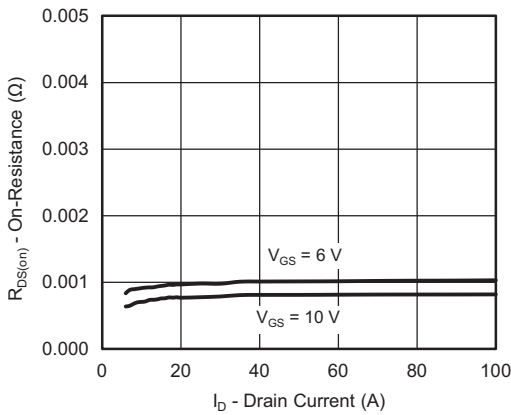
Transfer Characteristics



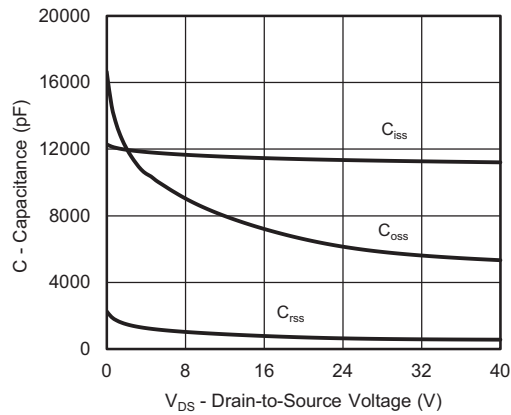
Transfer Characteristics



Transconductance

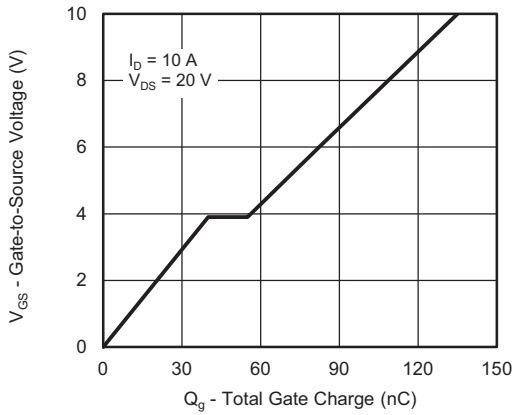


On-Resistance vs. Drain Current

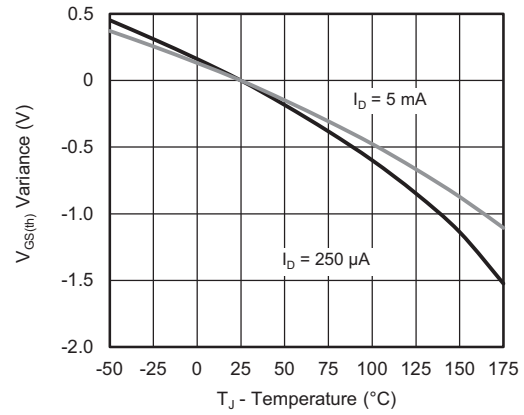


Capacitance

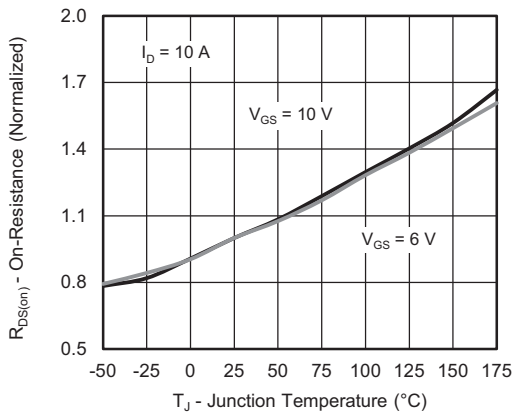
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



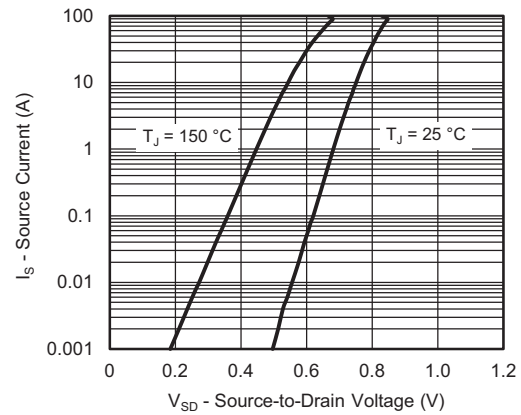
**Gate Charge**



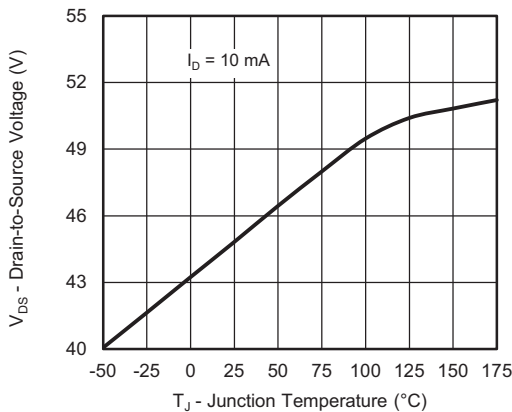
**Threshold Voltage**



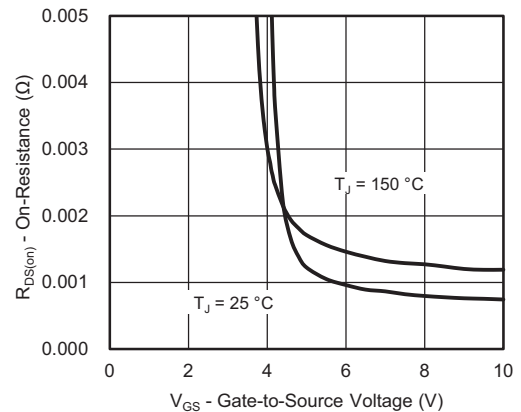
**On-Resistance vs. Junction Temperature**



**Source Drain Diode Forward Voltage**



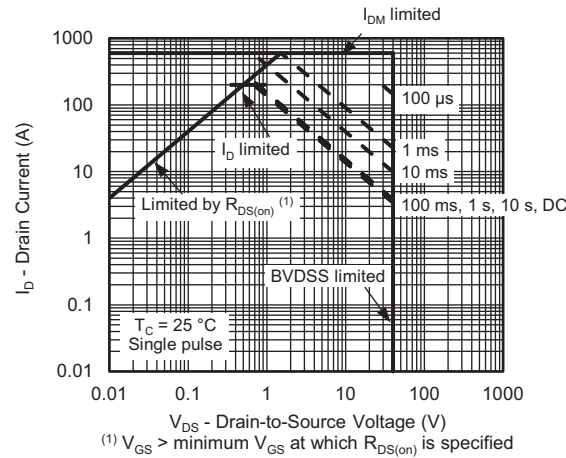
**Drain Source Breakdown vs. Junction Temperature**



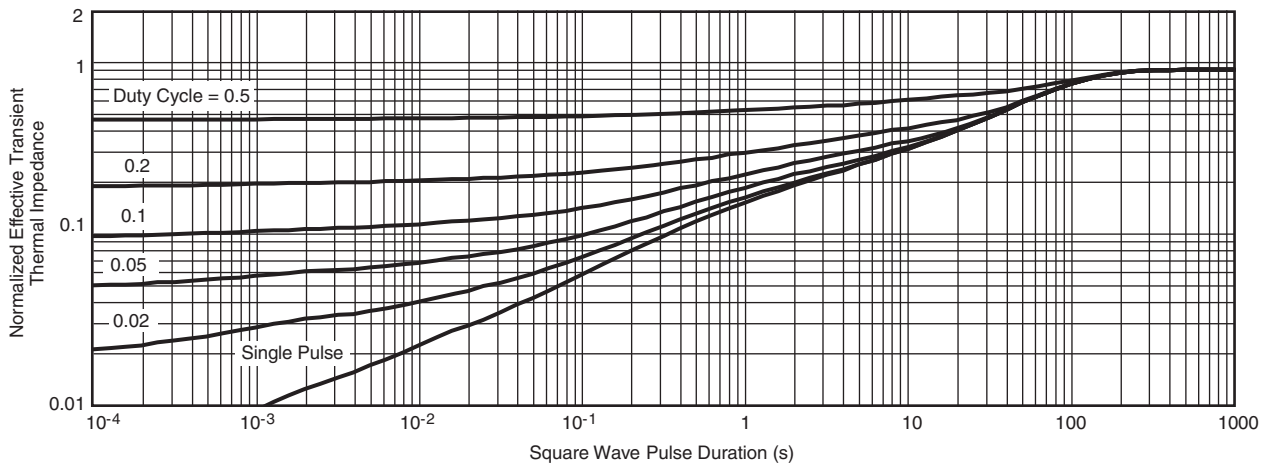
**On-Resistance vs. Gate-to-Source Voltage**



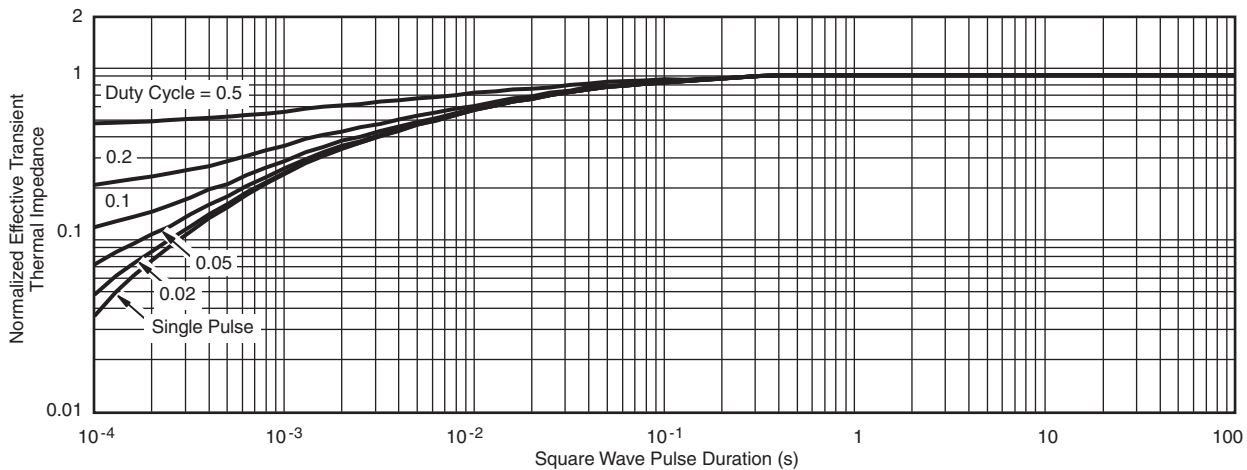
**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Safe Operating Area**



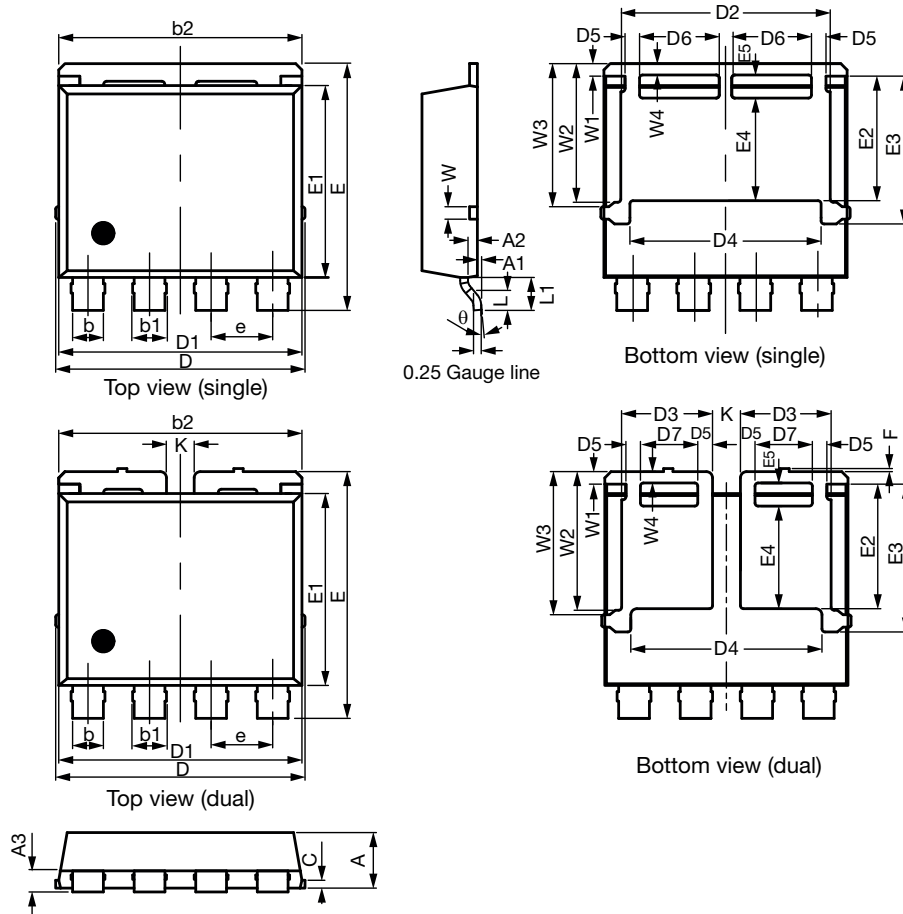
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?71828](http://www.vishay.com/ppg?71828).

## PowerPAK<sup>®</sup> 8 x 8L Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.70	1.80	1.90	0.067	0.071	0.075
A1	0.00	0.08	0.13	0.000	0.003	0.005
A2	0.25	0.30	0.35	0.010	0.012	0.014
A3	0.55	0.62	0.70	0.022	0.024	0.028
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	7.80	7.90	8.00	0.307	0.311	0.315
c	0.20	0.25	0.30	0.008	0.010	0.012
D	8.00	8.10	8.25	0.315	0.319	0.325
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D3	2.85	2.95	3.05	0.112	0.116	0.120
D4	6.11	6.21	6.31	0.241	0.244	0.248
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
D7	1.76	1.86	1.96	0.069	0.073	0.077



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	1.95	2.00	2.05	0.077	0.079	0.081
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	3.94	4.04	4.14	0.140	0.159	0.163
E3	4.69	4.79	4.89	0.185	0.189	0.193
E4	3.23	3.33	3.43	0.127	0.131	0.135
E5	0.65	0.75	0.85	0.026	0.030	0.033
F	0.00	0.10	0.15	0.000	0.004	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.80	0.90	1.00	0.031	0.035	0.039
W	0.30	0.40	0.50	0.012	0.016	0.020
W1	0.30	0.40	0.50	0.012	0.016	0.020
W2	4.39	4.49	4.59	0.173	0.177	0.181
W3	4.54	4.64	4.74	0.179	0.183	0.187
W4	0.32	0.37	0.42	0.013	0.015	0.017
θ	6°	10°	14°	6°	10°	14°

C17-1388-Rev. B, 16-Oct-17  
DWG: 6026



# Recommended Minimum PADS for PowerPAK<sup>®</sup> 8 x 8L Single



Dimensions in millimeters (inches)

**Note**

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.





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