

N-Channel 20-V (D-S) 175 °C MOSFET

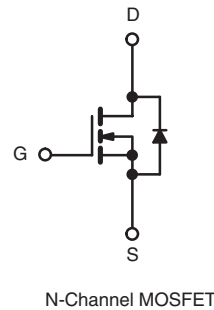
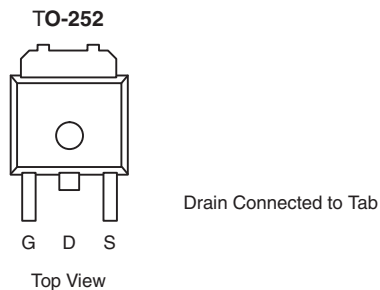
PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a
20	0.0095 at V _{GS} = 10 V	20
	0.017 at V _{GS} = 4.5 V	15

FEATURES

- TrenchFET[®] Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- 100 % R_g Tested

APPLICATIONS

- High-Side Synchronous Buck DC/DC Conversion
 - Desktop
 - Server



Ordering Information: SUD50N02-09P
SUD50N02-09P-E3 (Lead free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^a	I _D	T _A = 25 °C	20
		T _C = 100 °C	14
Pulsed Drain Current	I _{DM}	100	A
Continuous Source Current (Diode Conduction) ^a	I _S	4.3	
Avalanche Current	I _{AS}	29	
Single Pulse Avalanche Energy	E _{AS}	42	mJ
Maximum Power Dissipation	P _D	T _A = 25 °C	6.5 ^a
		T _C = 25 °C	39.5
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	19	23	°C/W
		Steady State	40	50	
Maximum Junction-to-Case	R _{thJC}	3.1	3.8		

Notes:

a. Surface Mounted on FR4 board, t ≤ 10 s.

b. Limited by package.



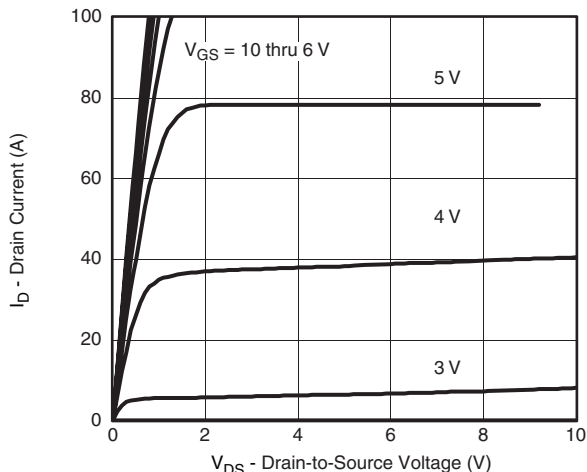
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.8		3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.008	0.0095	Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.014	
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0135	0.017	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	15			S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 10\text{ V}, f = 1\text{ MHz}$		1300		pF
Output Capacitance	C_{oss}			470		
Reverse Transfer Capacitance	C_{rss}			275		
Total Gate Charge ^c	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		10.5	16	nC
Gate-Source Charge ^c	Q_{gs}			4.2		
Gate-Drain Charge ^c	Q_{gd}			4.0		
Gate Resistance	R_g		1.6	4.0	6	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		8	12	ns
Rise Time ^c	t_r			10	15	
Turn-Off Delay Time ^c	$t_{d(off)}$			25	40	
Fall Time ^c	t_f			12	20	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}$						
Pulsed Current	I_{SM}				100	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 50\text{ A}, V_{GS} = 0\text{ V}$		1.2	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		35	70	ns

Notes:

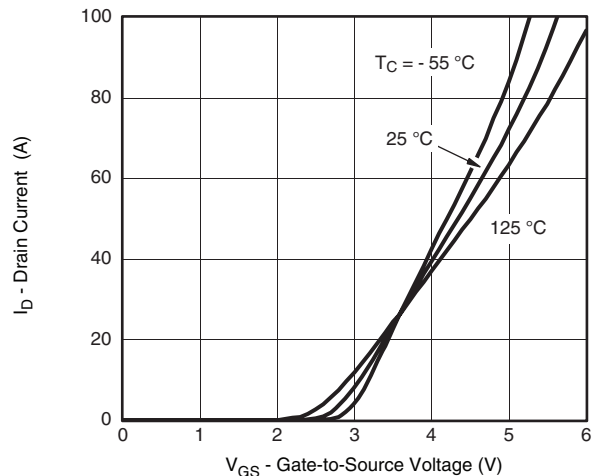
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

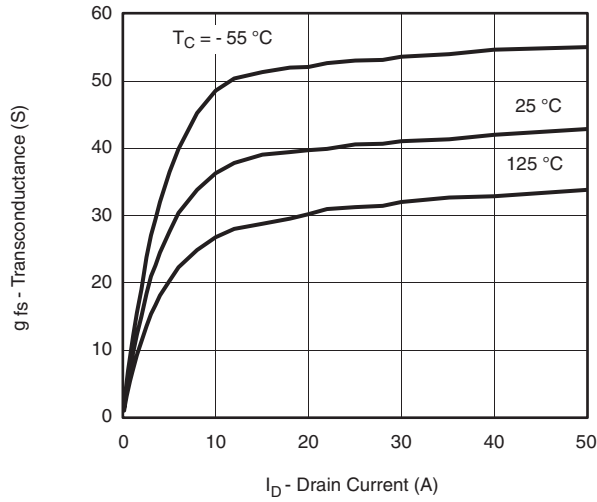
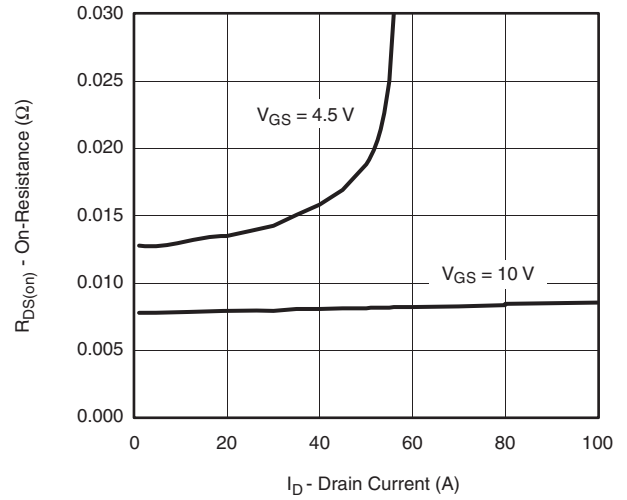
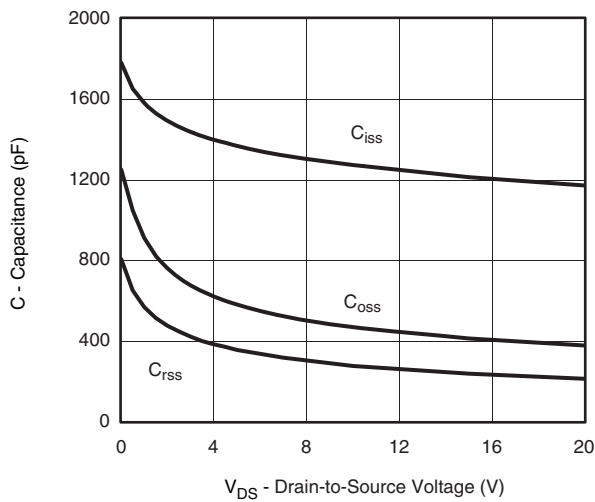
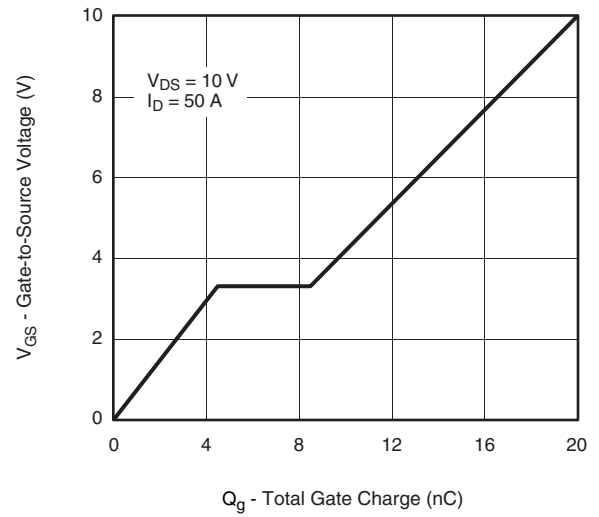
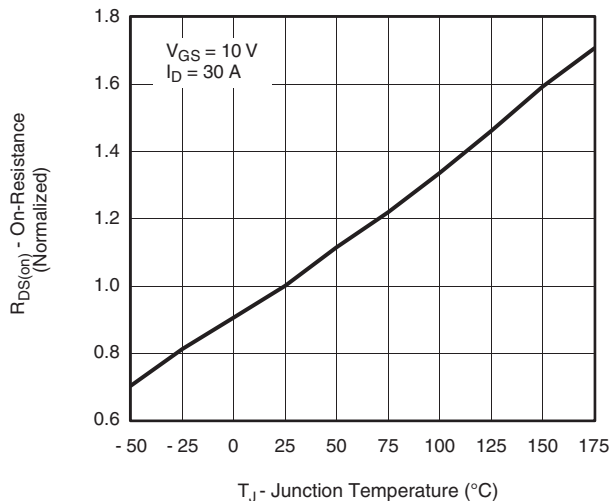
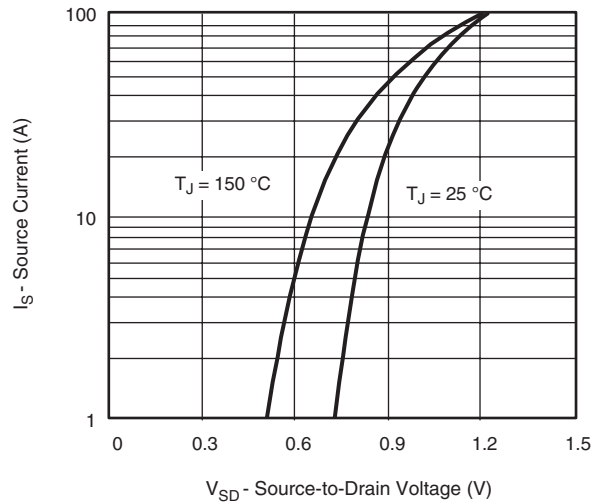
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



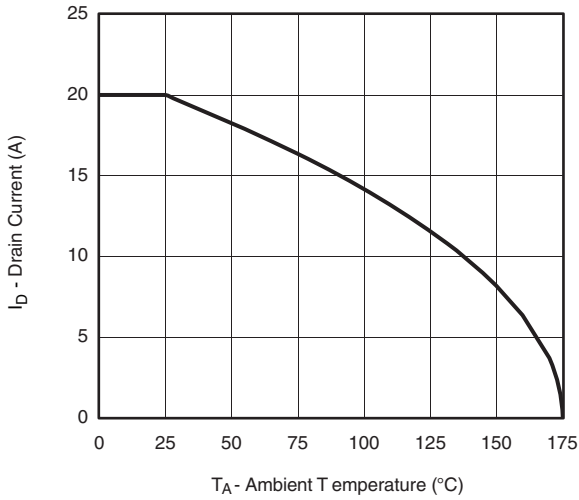
Output Characteristics



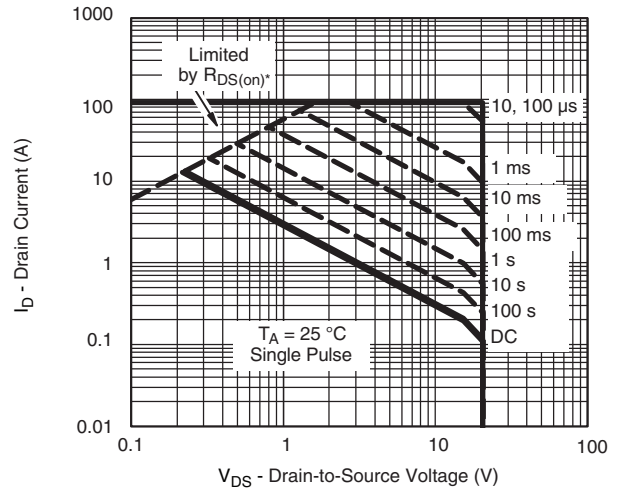
Transfer Characteristics

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

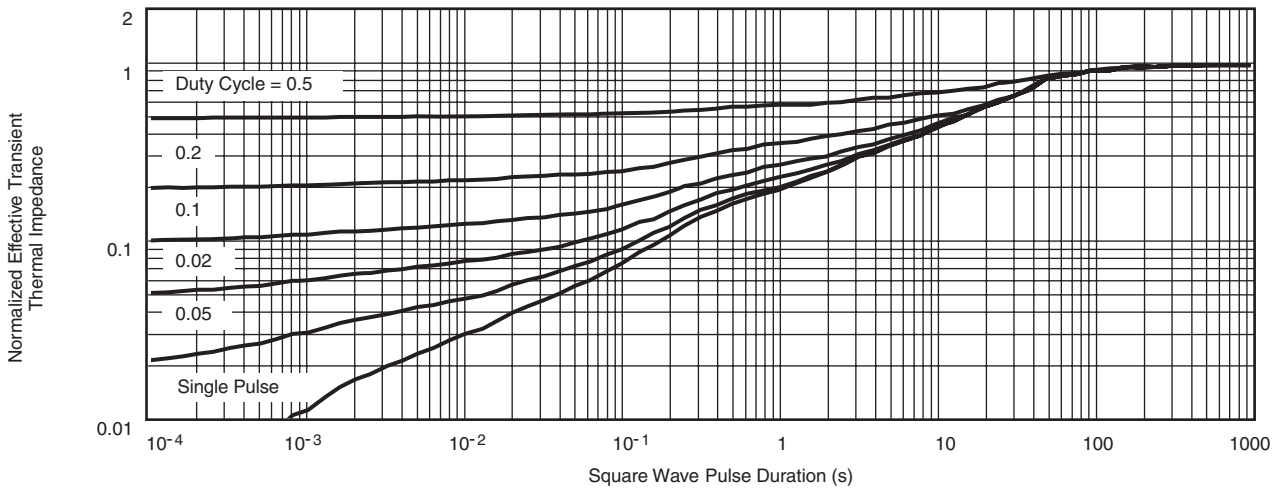
THERMAL RATINGS



Maximum Drain Current vs. Ambient Temperature



Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



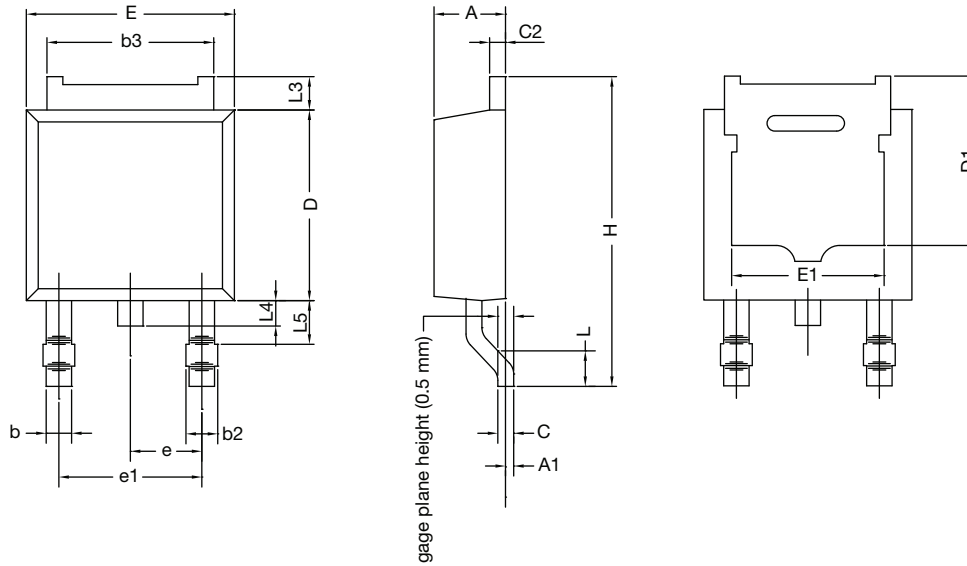
Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72034>.



TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



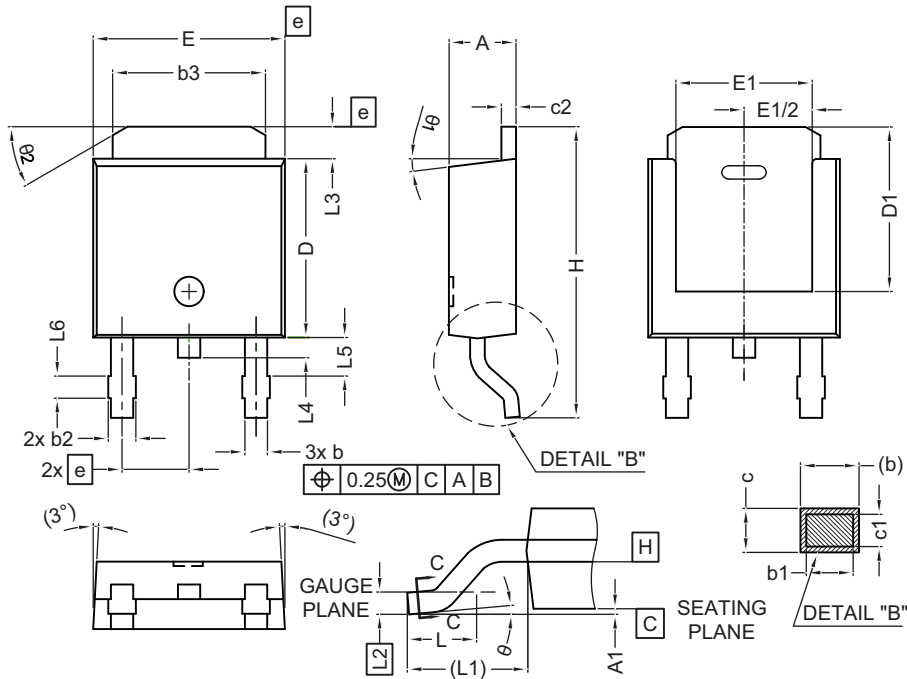
MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

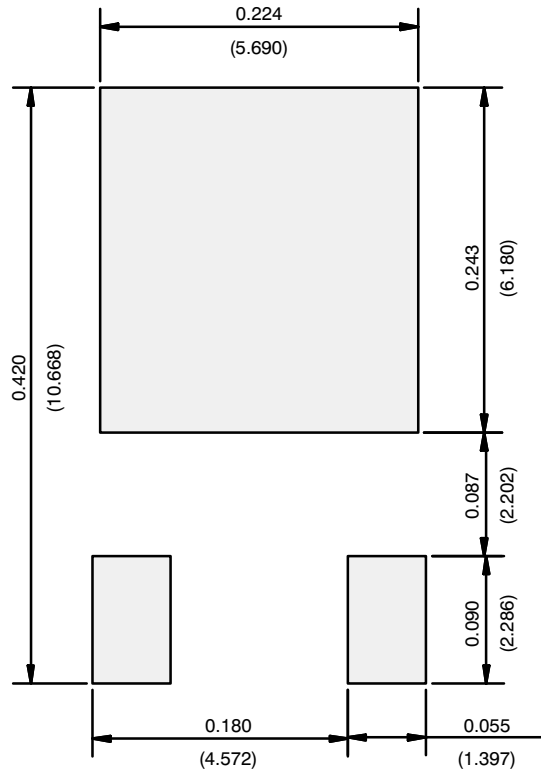
MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
 DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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