

N-Channel 30-V (D-S) MOSFET

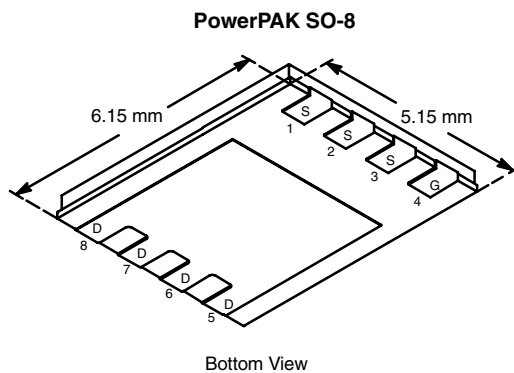
PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
30	0.003 @ $V_{GS} = 10$ V	30	45
	0.004 @ $V_{GS} = 4.5$ V	27	

FEATURES

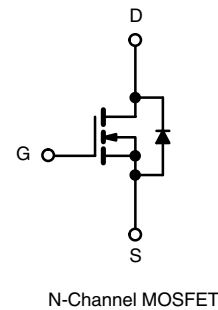
- Ultra-Low On-Resistance Using High Density TrenchFET® Gen II Power MOSFET Technology
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

APPLICATIONS

- Low-Side DC/DC Conversion
 - Notebook
 - Server
 - Workstation
- Point-of-Load Conversion



Ordering Information: Si7356DP-T1
Si7356DP-T1—E3 (Lead (Pb)-Free)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	10 secs	Steady State
Drain-Source Voltage		V_{DS}	30	
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	30	18
	$T_A = 70^\circ\text{C}$		25	15
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	70	
Continuous Source Current (Diode Conduction) ^a		I_S	4.5	1.8
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5.4	1.9
	$T_A = 70^\circ\text{C}$		3.4	1.2
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	18	23
	Steady State		50	65
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.5

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

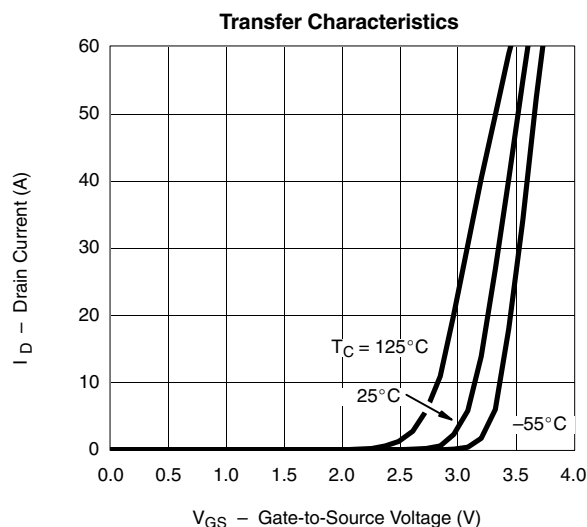
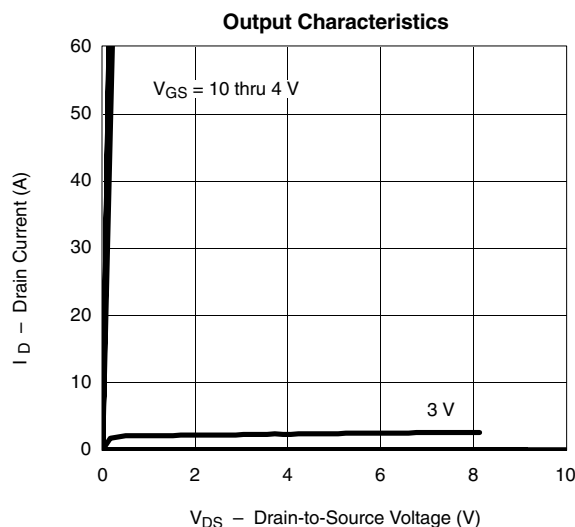
MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 25\ \text{A}$		0.0024	0.003	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 19\ \text{A}$		0.0032	0.004	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 25\ \text{A}$		110		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.72	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 20\ \text{A}$		45	70	nC
Gate-Source Charge	Q_{gs}			20		
Gate-Drain Charge	Q_{gd}			16		
Gate Resistance	R_g			1.1		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		27	40	ns
Rise Time	t_r			21	35	
Turn-Off Delay Time	$t_{d(off)}$			107	160	
Fall Time	t_f			43	65	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		45	70	

Notes

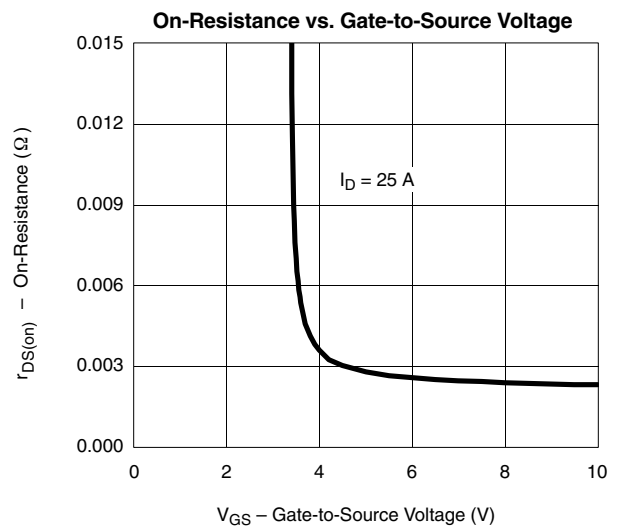
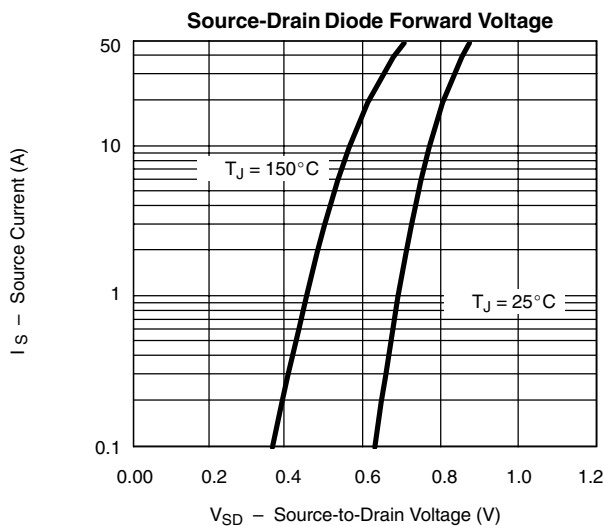
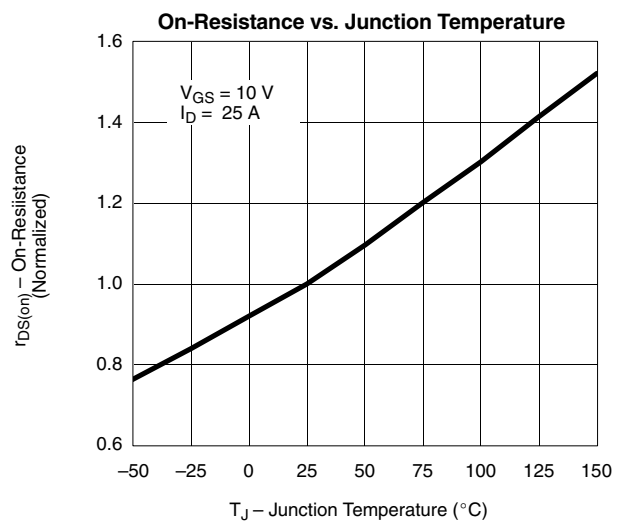
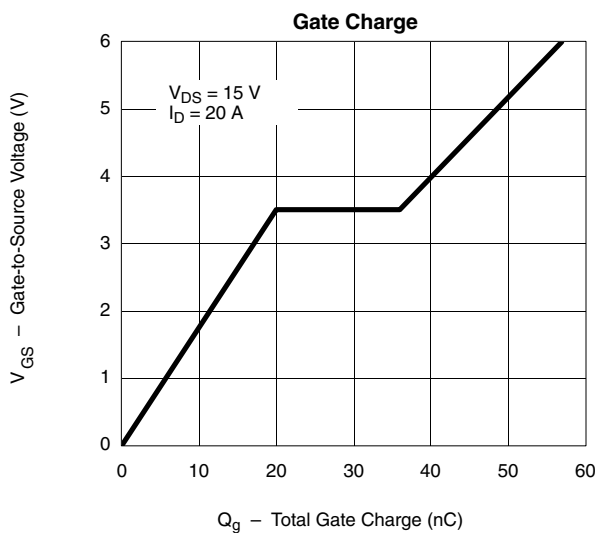
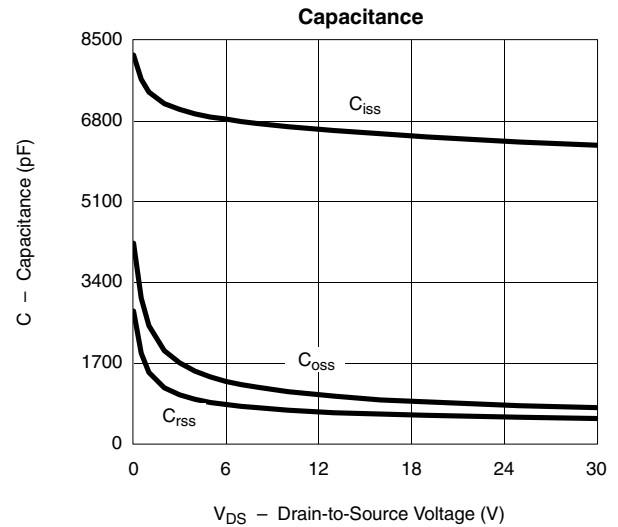
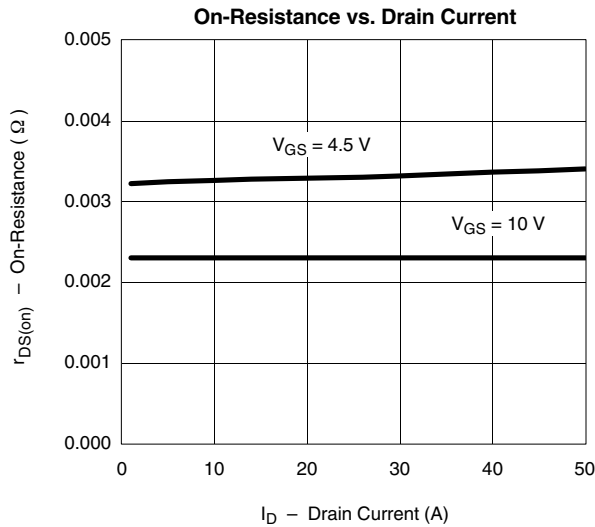
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

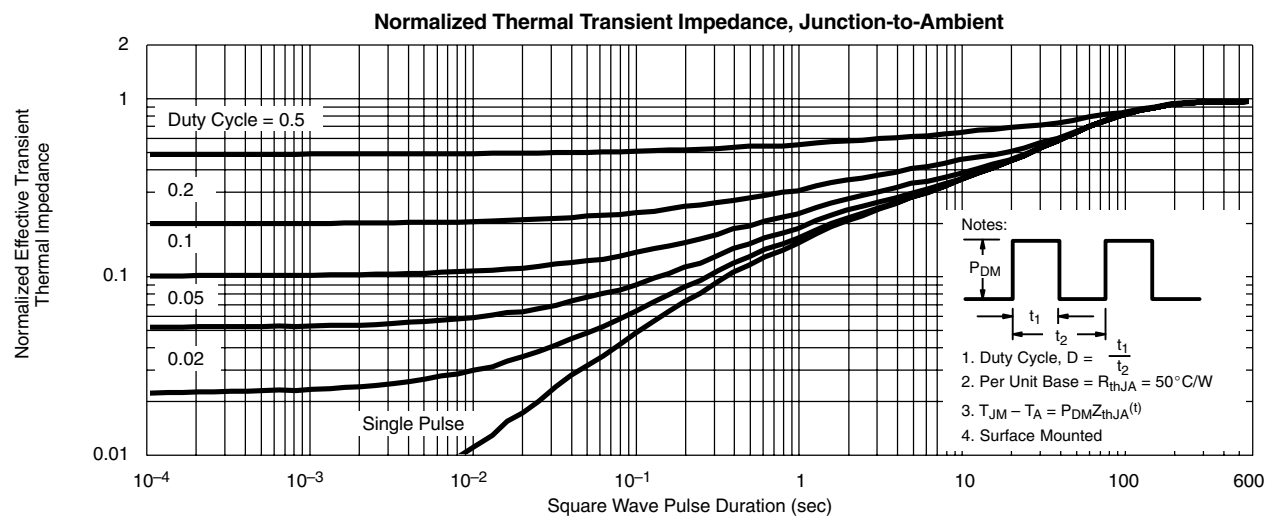
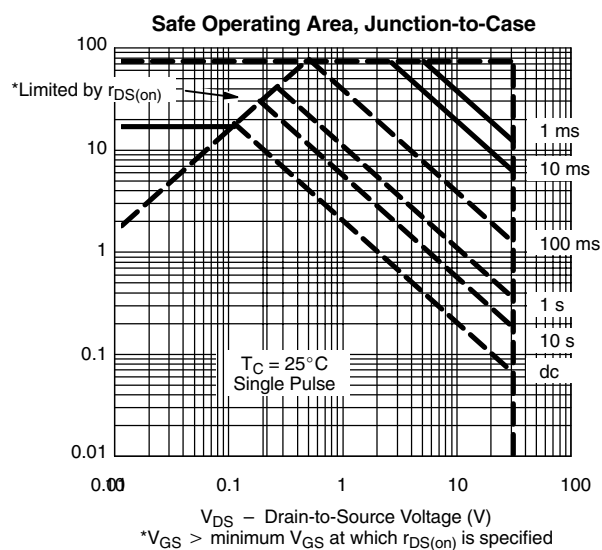
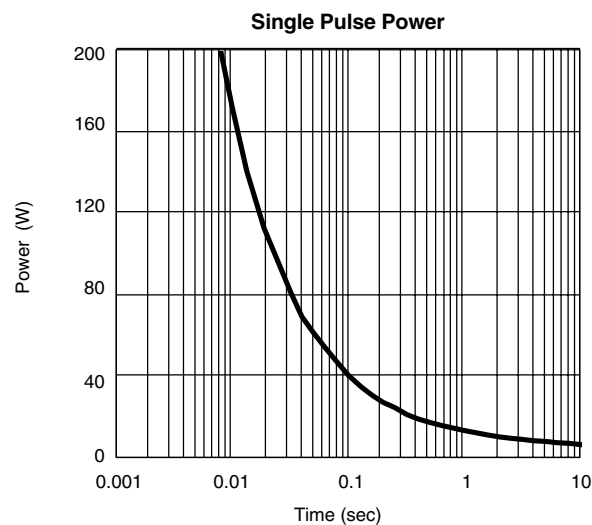
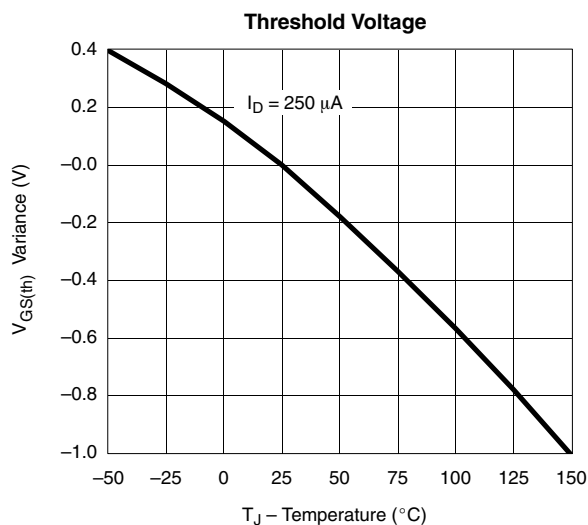
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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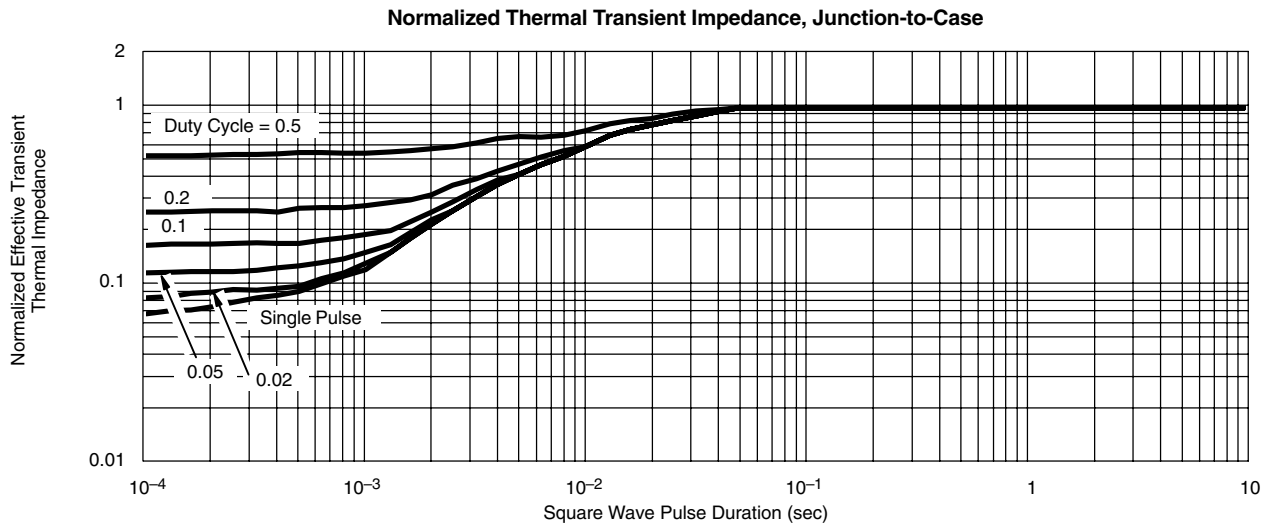


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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