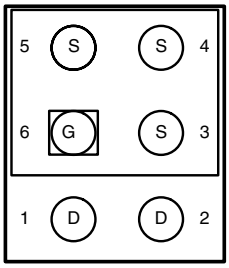
P-Channel 20 V (D-S) MOSFET

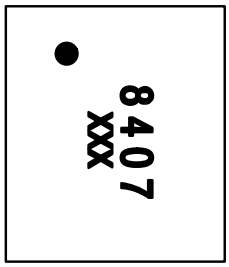
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.027 at V_{GS} = - 4.5 V	- 8.2
	0.032 at V_{GS} = - 2.5 V	- 7.5
	0.045 at V_{GS} = - 1.8 V	- 6.6

MICRO FOOT

Bump Side View



Backside View



Device Marking: 8407
xxx = Date/Lot Traceability Code

Ordering Information: Si8407DB-T2-E1 (Lead (Pb)-free and Halogen-free)

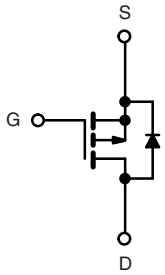
FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- MICRO FOOT® Chipscale Packaging Reduces Ultra-Low Footprint Area Profile (0.62 mm) and On-Resistance
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Portable Devices
  - PA Switch
  - Battery Switch
  - Load Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	- 20		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	- 8.2	- 5.8	A
	T_A = 70 °C		- 6.5	- 4.6	
Pulsed Drain Current		I_{DM}	- 15		
Continuous Source Current (Diode Conduction)[a]		I_S	- 2.6	- 1.34	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.9	1.47	W
	T_A = 70 °C		1.86	0.94	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Package Reflow Conditions[b]	IR/Convection		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	33	43	°C/W
	Steady State		72	85	
Maximum Junction-to-Foot (drain)	Steady State	R_{thJF}	15	19	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.

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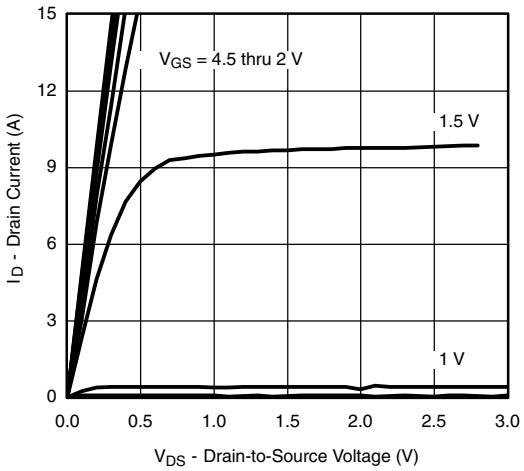
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 350 µA	- 0.4		- 0.9	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 70 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 1 A		0.022	0.027	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.026	0.032	
		V_{GS} = - 1.8 V, I_D = - 1 A		0.033	0.045	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 1 A		10		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 1 A, V_{GS} = 0		- 0.6	- 1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 1 A		32	50	nC
Gate-Source Charge	Q_{gs}			3.6		
Gate-Drain Charge	Q_{gd}			8.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		30	45	ns
Rise Time	t_r			45	70	
Turn-Off Delay Time	$t_{d(off)}$			550	825	
Fall Time	t_f			220	330	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 1 A, dI/dt = 100 A/µs		265	500	

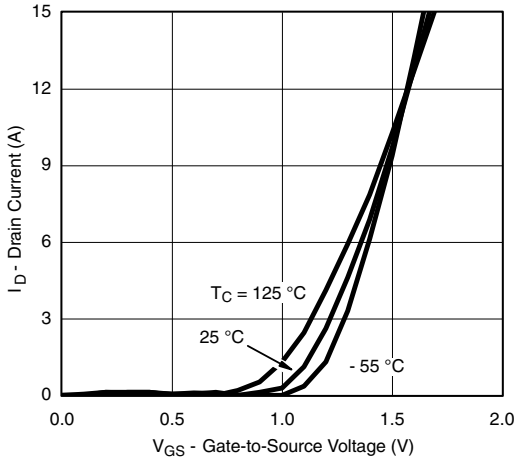
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Output Characteristics



Transfer Characteristics

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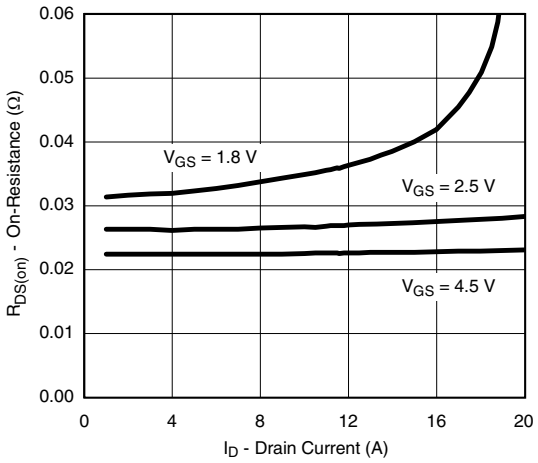
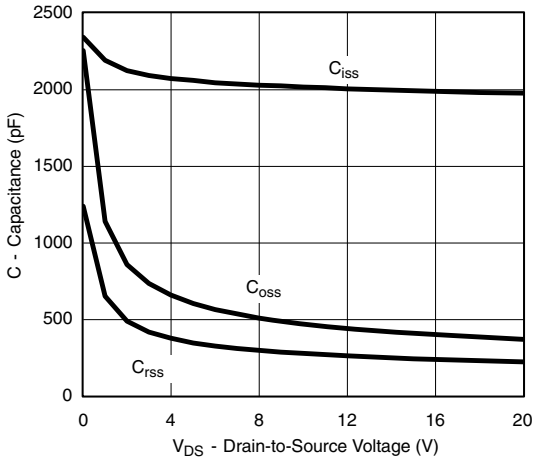
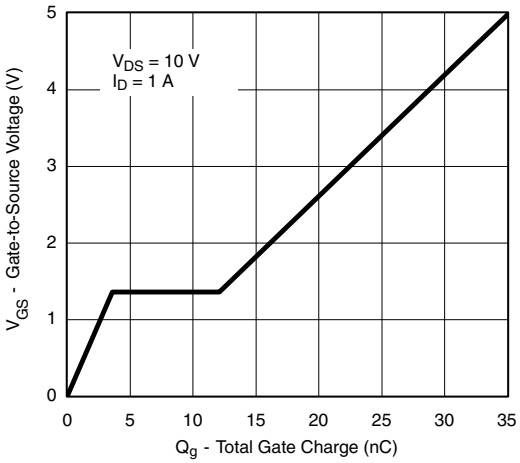
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



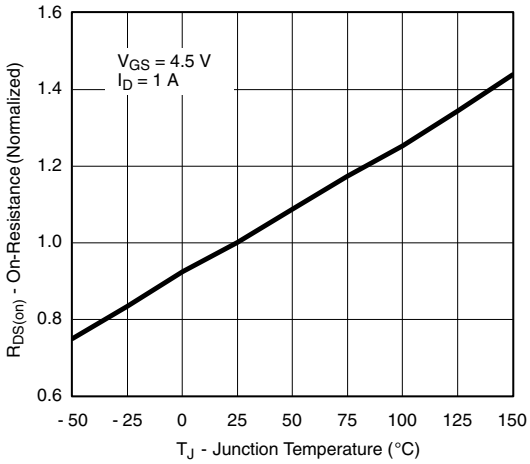
On-Resistance vs. Drain Current



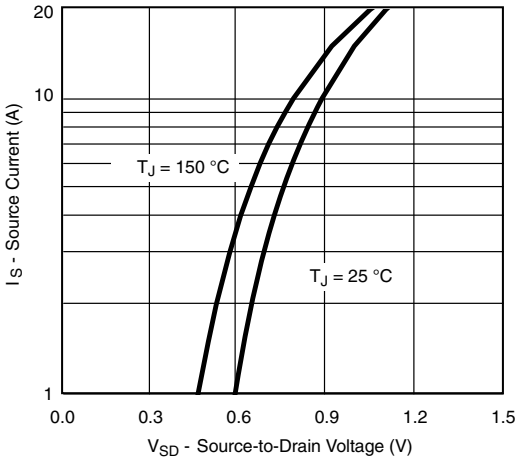
Capacitance



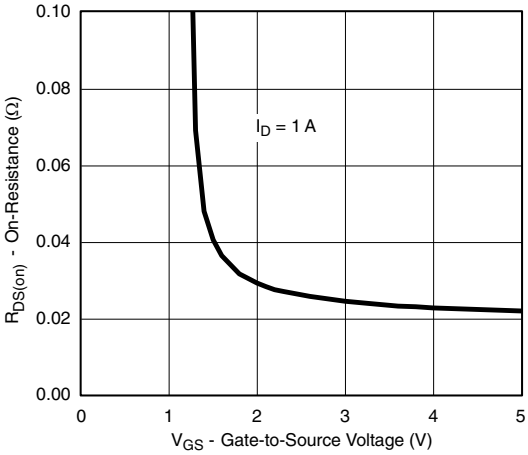
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

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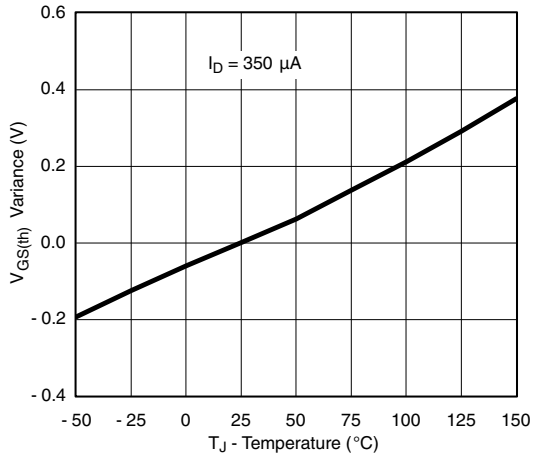
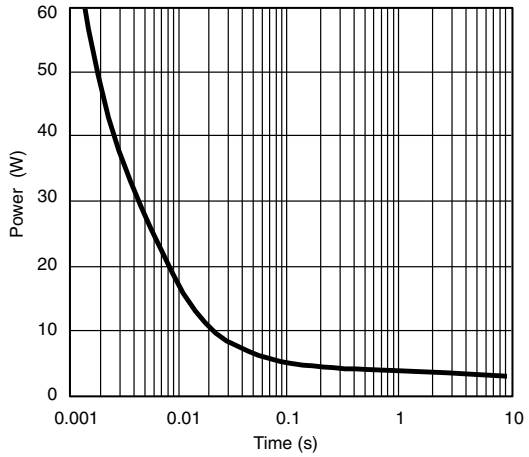
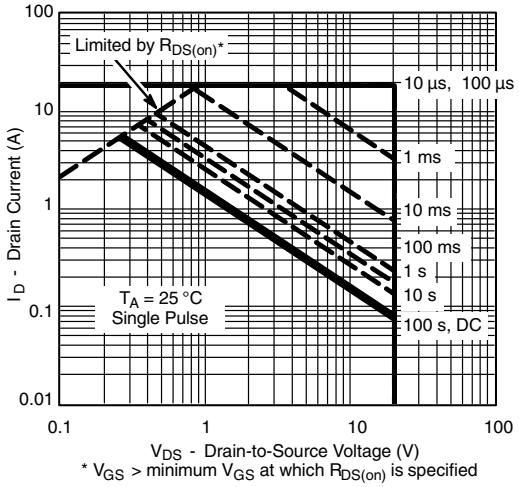


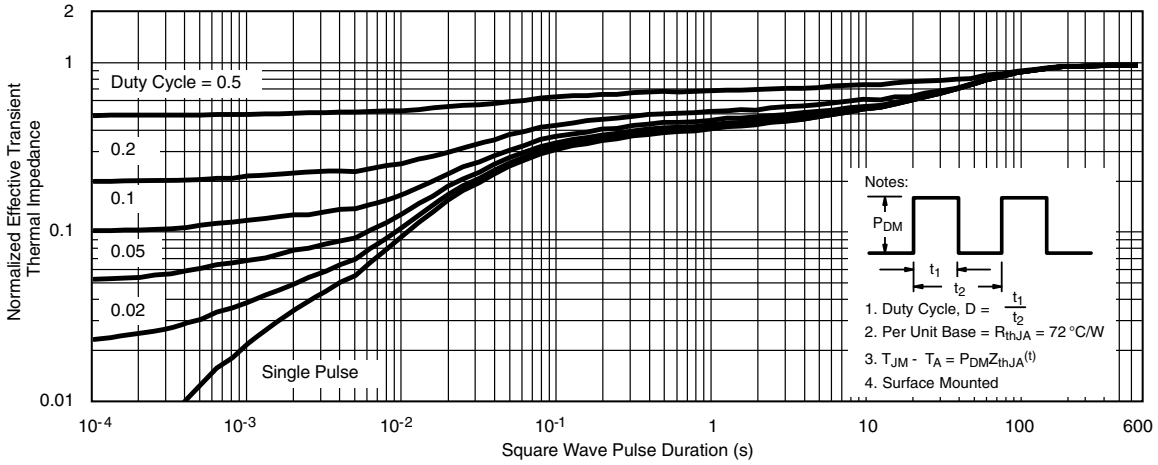
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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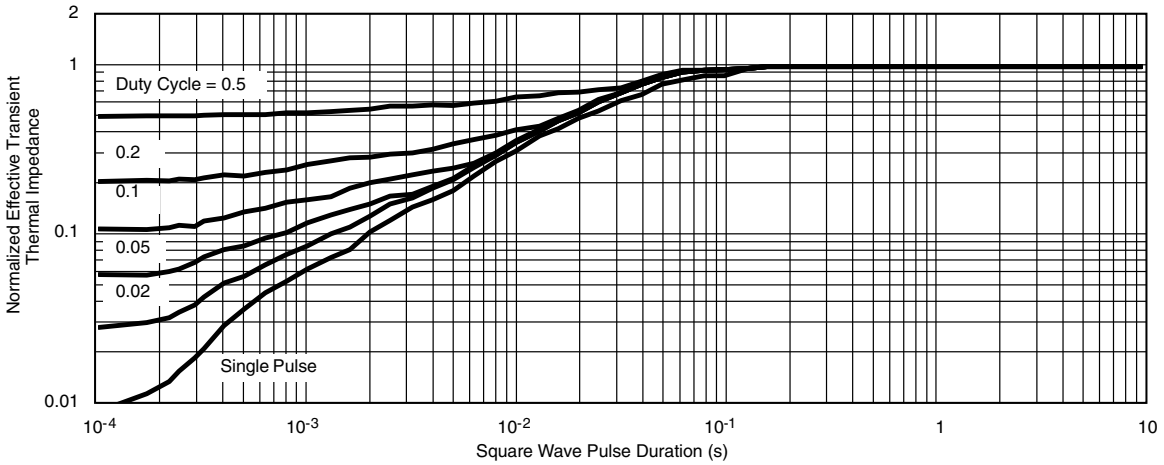
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

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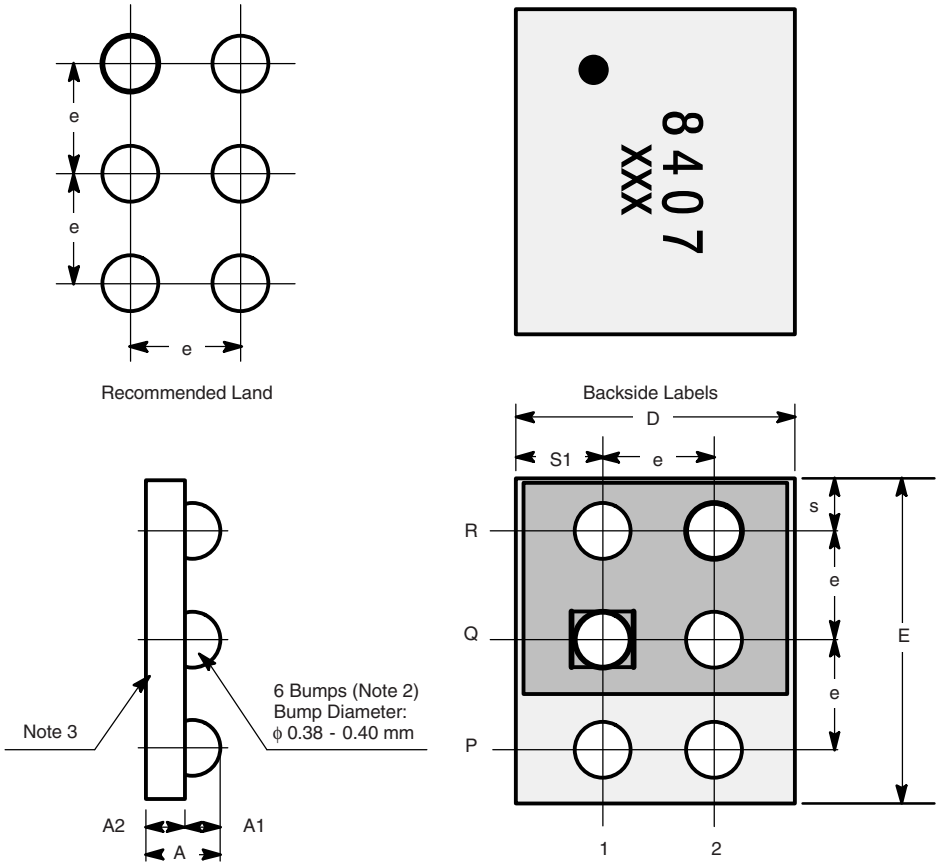
PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (2.4 mm x 2 mm, 0.8 mm PITCH)



Notes (Unless Otherwise Specified):
1. All dimensions are in millimeters.
2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu with diameter ϕ 0.38 mm - 0.40 mm.
3. Backside surface is coated with a Ti/Nl/Ag layer.
4. Non-solder mask defined copper landing pad.
5. The flat side of wafers is oriented at the bottom.
6. • is location of Pin 1P.

Dim.	Millimeters[a]		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.0102	0.0114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.920	2.000	0.0756	0.0787
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
S	0.370	0.400	0.0150	0.0157
S1	0.580	0.600	0.0228	0.0236

Notes:
a. Use millimeters as the primary measurement.

PAD DISTRIBUTION TABLE			
	P	Q	R
1	Drain	Gate	Source
2	Drain	Source	Source

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