Dual P-Channel 30-V/20-V (D-S) MOSFET

CHARACTERISTICS

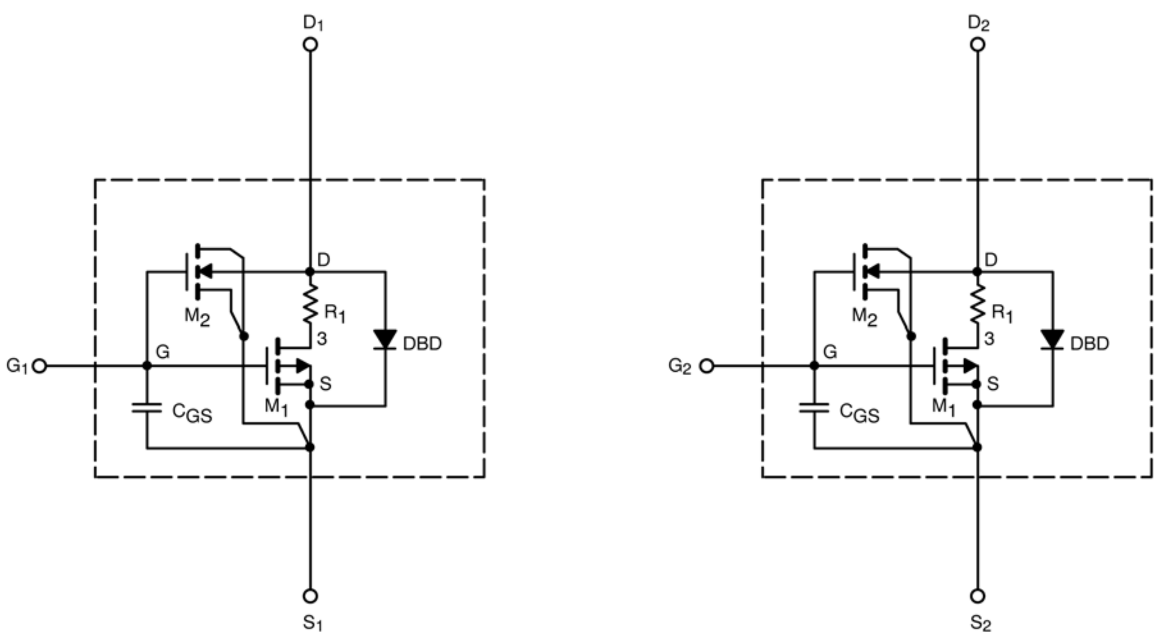
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



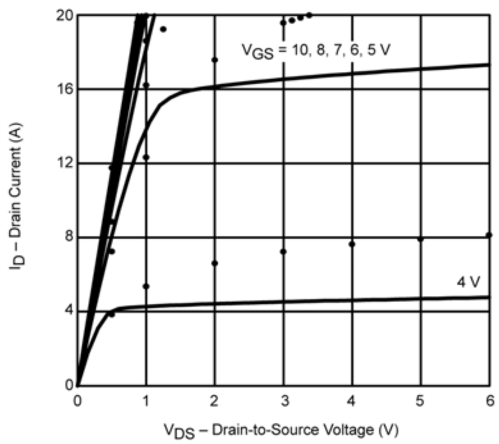
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

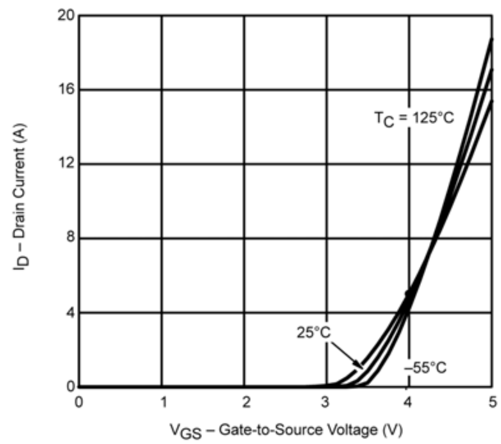
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –250 µA	Ch 1	2.6		V
		$V_{DS} = V_{GS}$, I_D = –250 µA	Ch 2	0.70		
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = – 10 V	Ch 1	101		A
		V_{DS} = –5 V, V_{GS} = –4.5 V	Ch 2	113		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –5 A	Ch 1	0.044	0.044	Ω
		V_{GS} = –4.5 V, I_D = –7 A	Ch 2	0.022	0.022	
		V_{GS} = –4.5 V, I_D = –3.7 A	Ch 1	0.067	0.082	
		V_{GS} = –2.5 V, I_D = –6.2 A	Ch 2	0.027	0.029	
		V_{GS} = –1.8 V, I_D = –3 A	Ch 2	0.034	0.039	
Forward Transconductance[a]	g_{fs}	V_{DS} = –15 V, I_D = –5 A	Ch 1	11	15	S
		V_{DS} = –15 V, I_D = –3 A	Ch 2	10	9	
Diode Forward Voltage[a]	V_{SD}	I_S = –1.7 A, V_{GS} = 0 V	Ch 1	0.80	0.80	V
		I_S = –1.7 A, V_{GS} = 0 V	Ch 2	0.80	–0.80	
Dynamic[b]						
Total Gate Charge	Q_g	P-Channel 1 V_{DS} = –15 V, V_{GS} = –10 V, I_D = –5 A P-Channel 2 V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –7 A	Ch 1	12	12.5	nC
			Ch 2	21.7	21	
Gate-Source Charge	Q_{gs}		Ch 1	2.1	2.1	
			Ch 2	2.6	2.6	
Gate-Source Charge	Q_{gs}		Ch 1	3.5	3.5	
			Ch 2	6	6	
Turn-On Delay Time	$t_{d(on)}$	P-Channel 1 V_{DD} = –15 V, R_L = 15 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω P-Channel 2 V_{DD} = –15 V, R_L = 15 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω	Ch 1	11	7	ns
			Ch 2	32	20	
Rise Time	t_r		Ch 1	8	10	
			Ch 2	13	40	
Turn-Off Delay Time	$t_{d(off)}$		Ch 1	8	30	
			Ch 2	55	125	
Fall Time	t_f		Ch 1	9	22	
			Ch 2	17	85	

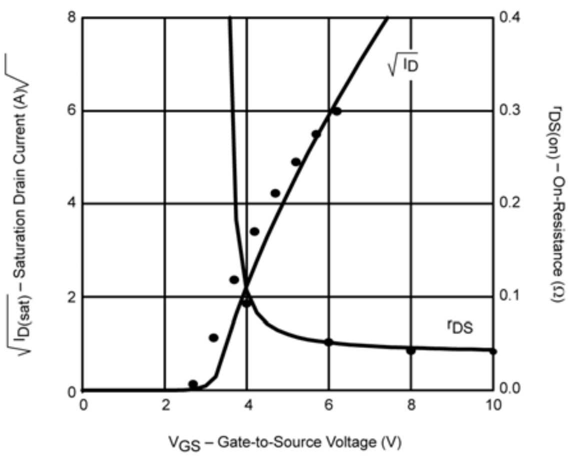
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

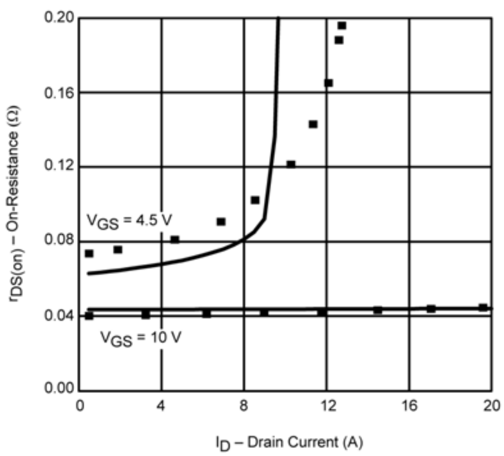
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

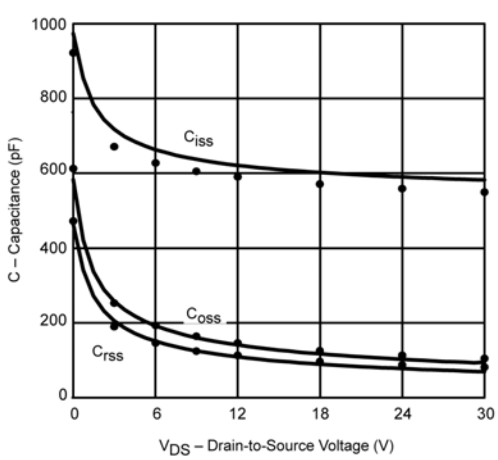
Channel 1

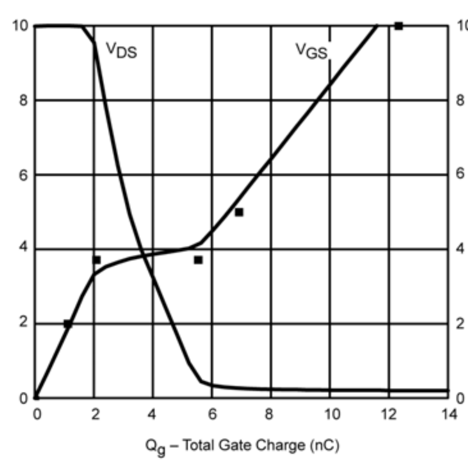






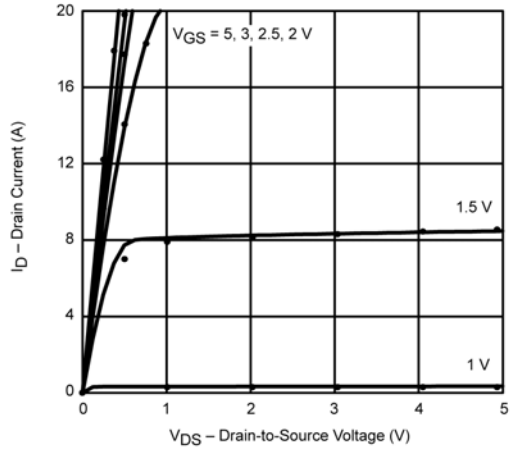


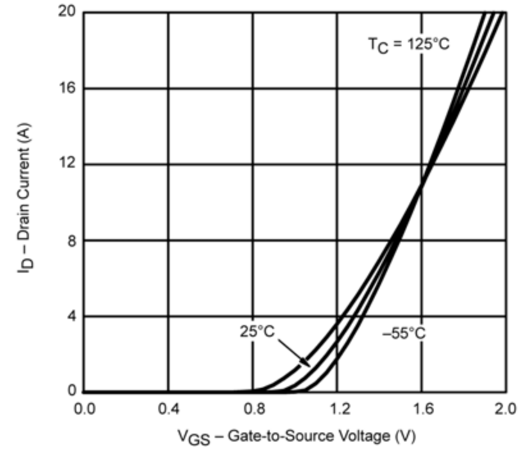


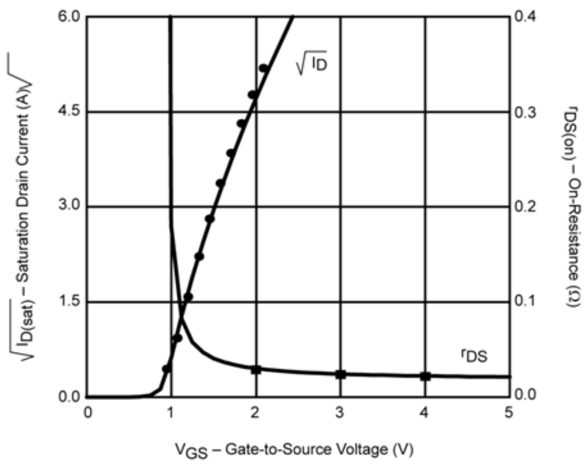


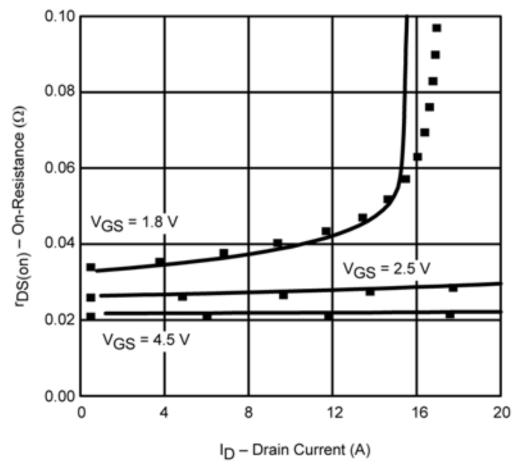
Note: Dots and squares represent measured data.

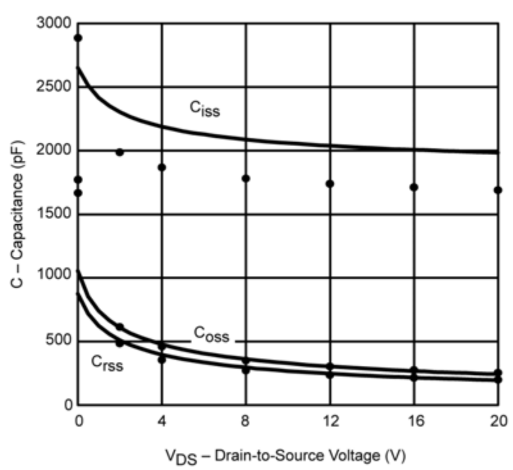
Channel 2

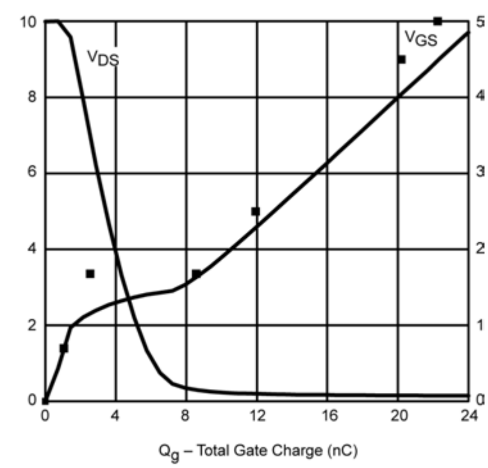












Note: Dots and squares represent measured data.

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