

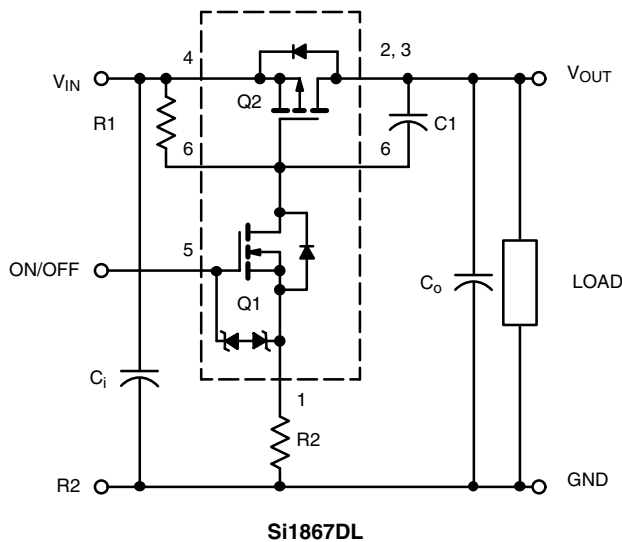
Load Switch with Level-Shift

PRODUCT SUMMARY		
V _{DS2} (V)	R _{DS(on)} (Ω)	I _D (A)
1.8 to 8	0.600 at V _{IN} = 4.5 V	± 0.6
	0.850 at V _{IN} = 2.5 V	± 0.5
	1.200 at V _{IN} = 1.8 V	± 0.2

DESCRIPTION

The Si1867DL includes a p- and n-channel MOSFET in a single SC70-6 package. The low on-resistance p-channel TrenchFET is tailored for use as a load switch. The n-Channel, with an external resistor, can be used as a level-shift to drive the P-Channel load-switch. The n-channel MOSFET has internal ESD protection and can be driven by logic signals as low as 1.5 V. The Si1867DL operates on supply lines from 1.8 V to 8 V, and can drive loads up to 0.6 A.

APPLICATION CIRCUITS



FEATURES

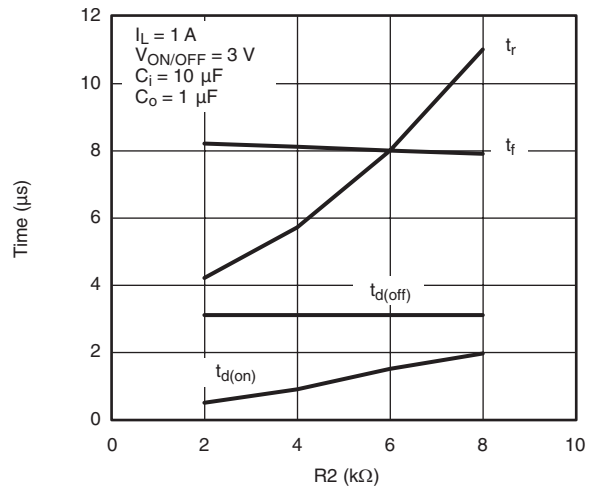
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 600 mΩ Low R_{DS(on)}
- 1.8 V to 8 V Input
- 1.5 V to 8 V Logic Level Control
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch with Level-Shift for Portable Applications



Note: For R2 switching variations with other V_{IN}/R1 combinations see Typical Characteristics

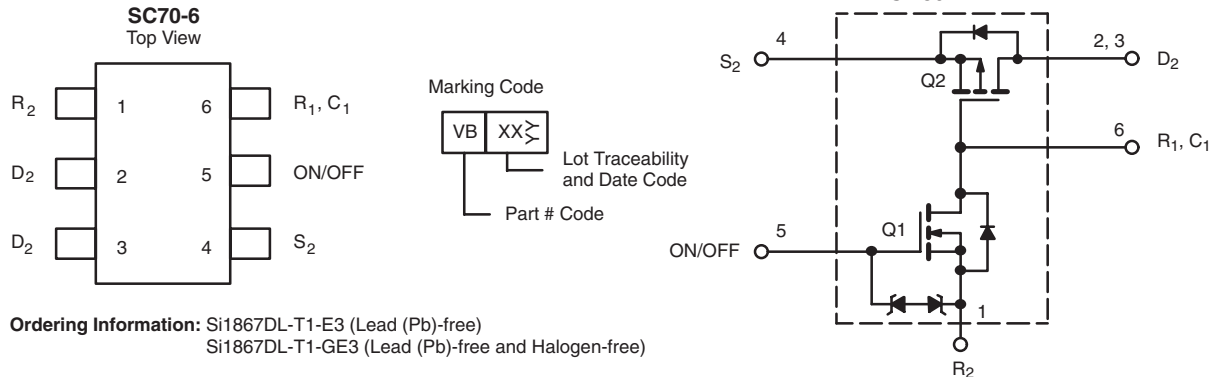
Switching Variation
R2 at V_{IN} = 2.5 V, R1 = 20 kΩ

COMPONENTS		
R1	Pull-Up Resistor	Typical 10 kΩ to 1 mΩ*
R2	Optional Slew-Rate Control	Typical 0 to 100 kΩ*
C1	Optional Slew-Rate Control	Typical 1000 pF

* Minimum R1 value should be least 10 x R2 to ensure Q1 turn-on.

The Si1867DL is ideally suited for high-side load switching in portable applications. The integrated n-channel level-shift devices saves space by reducing external components. The slew rate is set externally so that rise-times can be tailored to different load types.

FUNCTIONAL BLOCK DIAGRAM



Ordering Information: Si1867DL-T1-E3 (Lead (Pb)-free)
Si1867DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Input Voltage	V_{IN}	8	V
ON/OFF Voltage	$V_{ON/OFF}$	8	
Load Current	Continuous ^{a, b}	± 0.6	A
	Pulsed ^{b, c}	± 3	
Continuous Intrinsic Diode Conduction ^a	I_S	- 0.4	
Maximum Power Dissipation ^a	P_D	0.4	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
ESD Rating, MIL-STD-883C Human Body Model (100 pF, 1500 Ω)	ESD	2	kV

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (Continuous Current) ^a	R_{thJA}	260	320	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Foot (Q2)	R_{thJF}	190	230	

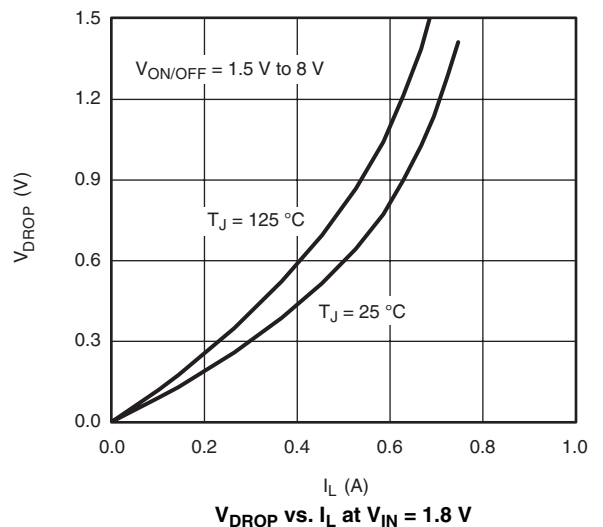
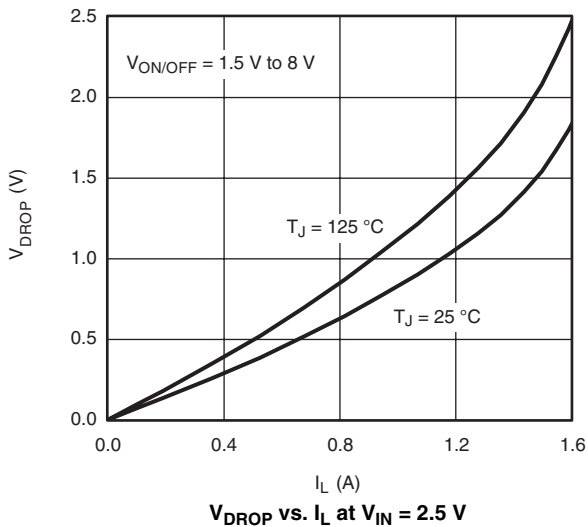
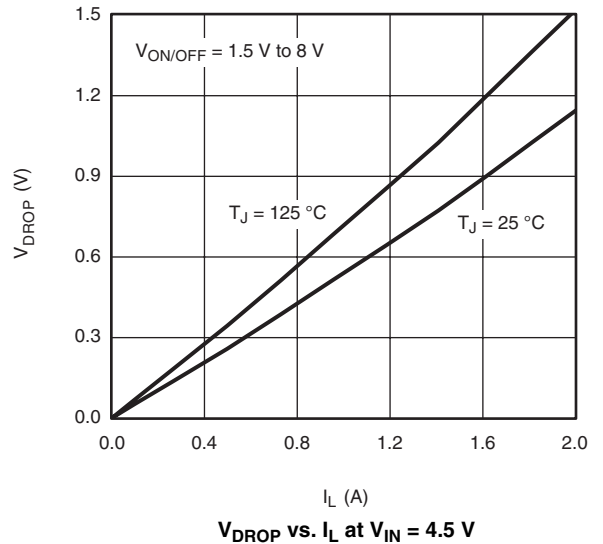
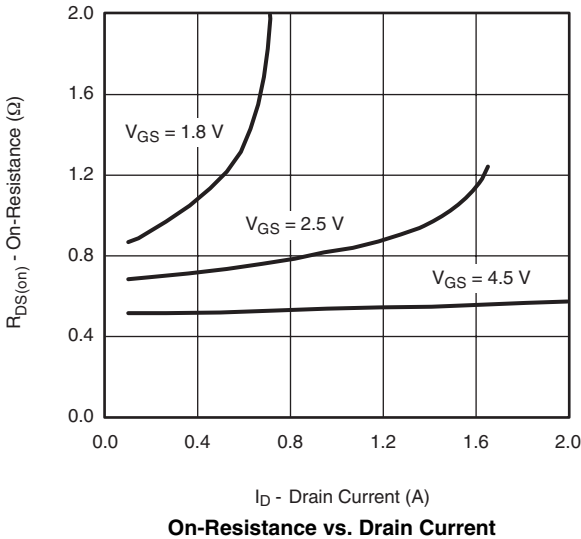
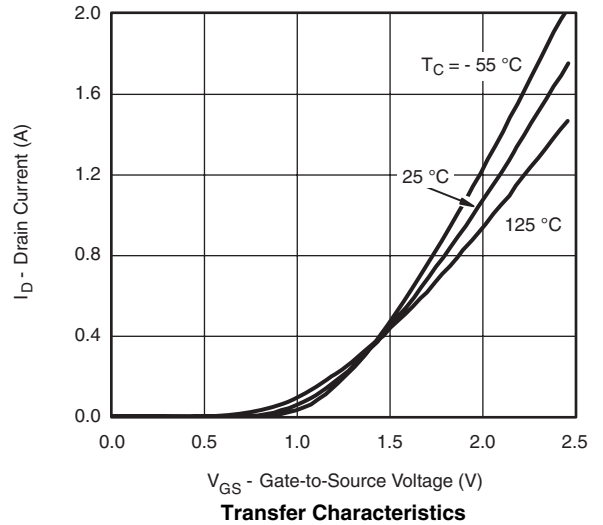
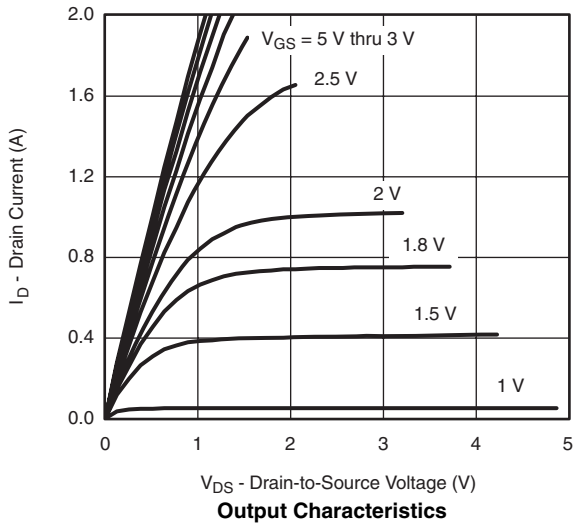
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OFF Characteristics						
Reverse Leakage Current	I_{FL}	$V_{IN} = 8\text{ V}, V_{ON/OFF} = 0\text{ V}$			1	μA
Diode Forward Voltage	V_{SD}	$I_S = -0.4\text{ A}$		0.85	1.1	V
ON Characteristics						
Input Voltage	V_{IN}		1.8		8	V
On-Resistance (P-Channel) at 1 A	$R_{DS(on)}$	$V_{ON/OFF} = 1.5\text{ V}, V_{IN} = 4.5\text{ V}, I_D = 0.6\text{ A}$		0.480	0.600	Ω
		$V_{ON/OFF} = 1.5\text{ V}, V_{IN} = 2.5\text{ V}, I_D = 0.5\text{ A}$		0.690	0.850	
		$V_{ON/OFF} = 1.5\text{ V}, V_{IN} = 1.8\text{ V}, I_D = 0.2\text{ A}$		0.950	1.200	
On-State (P-Channel) Drain-Current	$I_{D(on)}$	$V_{IN-OUT} \leq 0.2\text{ V}, V_{IN} = 5\text{ V}, V_{ON/OFF} = 1.5\text{ V}$	1			A
		$V_{IN-OUT} \leq 0.3\text{ V}, V_{IN} = 3\text{ V}, V_{ON/OFF} = 1.5\text{ V}$	1			

Notes:

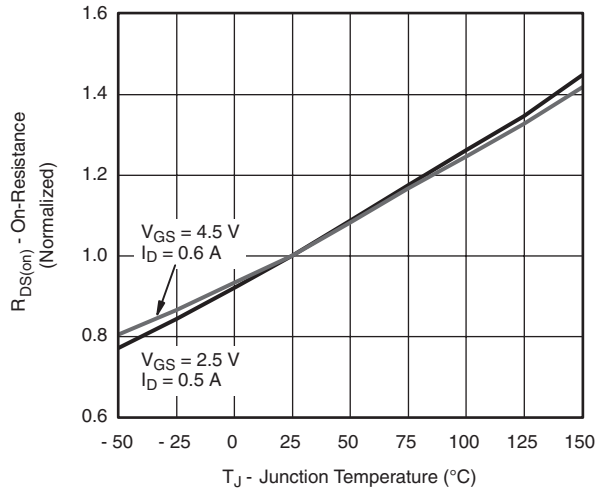
- a) Surface mounted on FR4 board.
- b) $V_{IN} = 8\text{ V}, V_{ON/OFF} = 8\text{ V}, T_A = 25\text{ }^\circ\text{C}$.
- c) Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

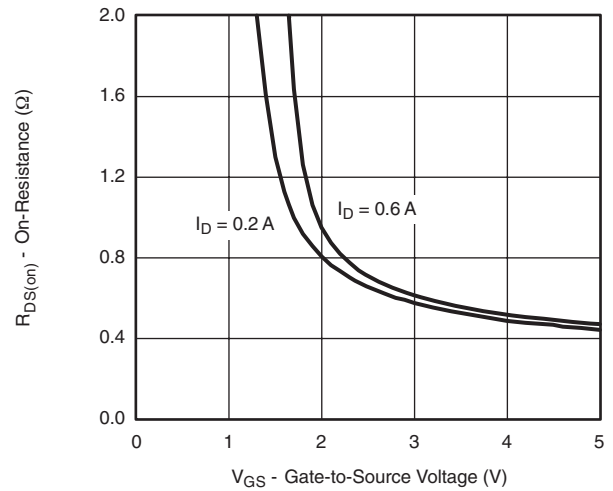
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



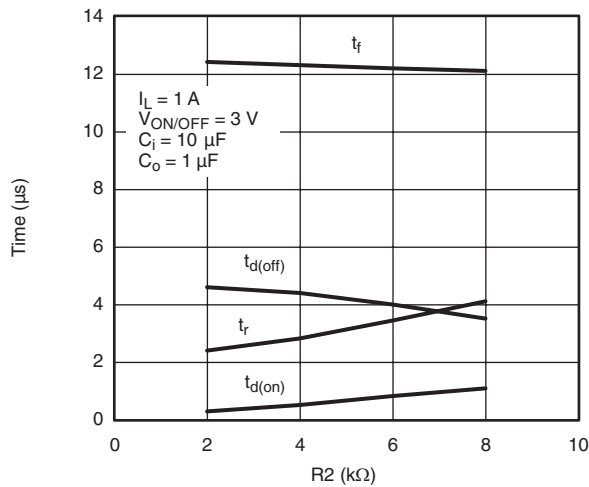
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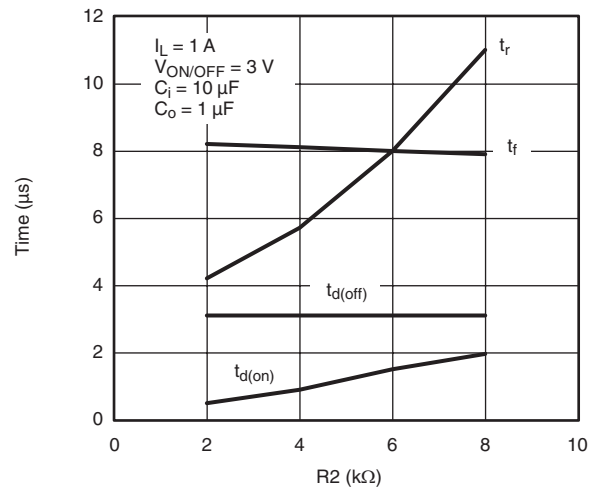
On Resistance vs. Junction Temperature



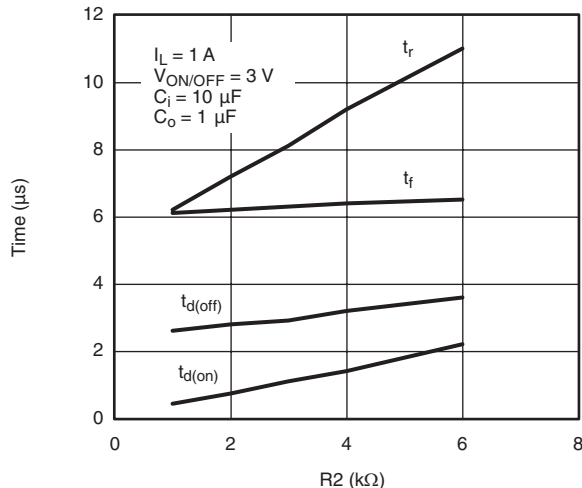
On-Resistance vs. Gate-to-Source Voltage



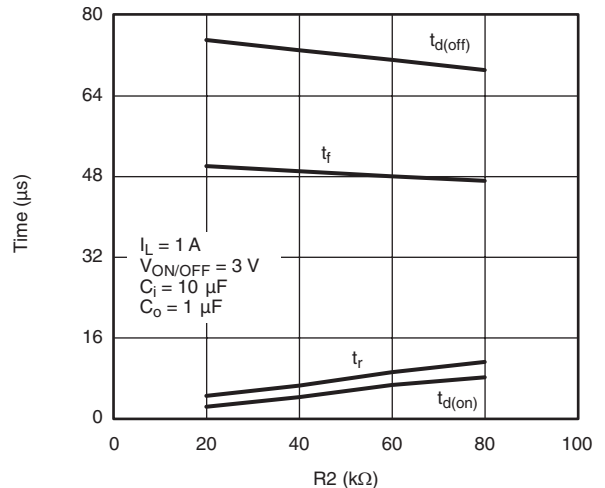
**Switching Variation
R2 at V_{IN} = 4.5 V, R1 = 20 kΩ**



**Switching Variation
R2 at V_{IN} = 2.5 V, R1 = 20 kΩ**

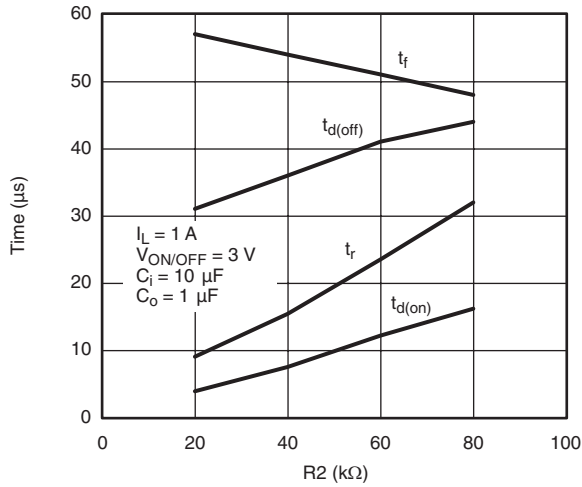


**Switching Variation
R2 at V_{IN} = 1.8 V, R1 = 20 kΩ**

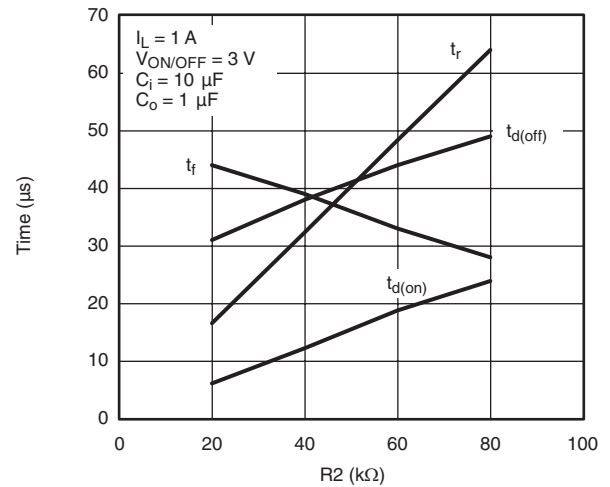


**Switching Variation
R2 at V_{IN} = 4.5 V, R1 = 300 kΩ**

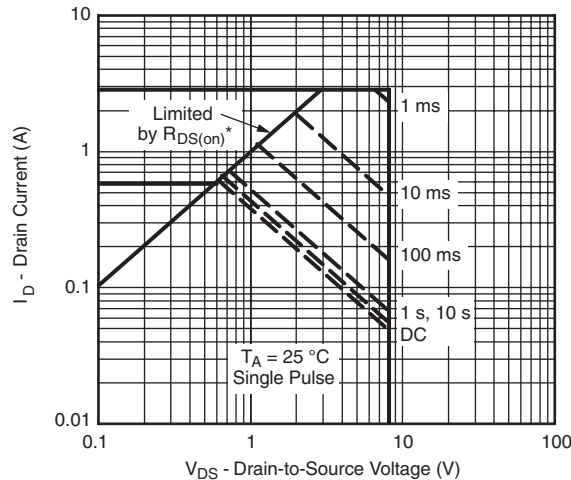
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



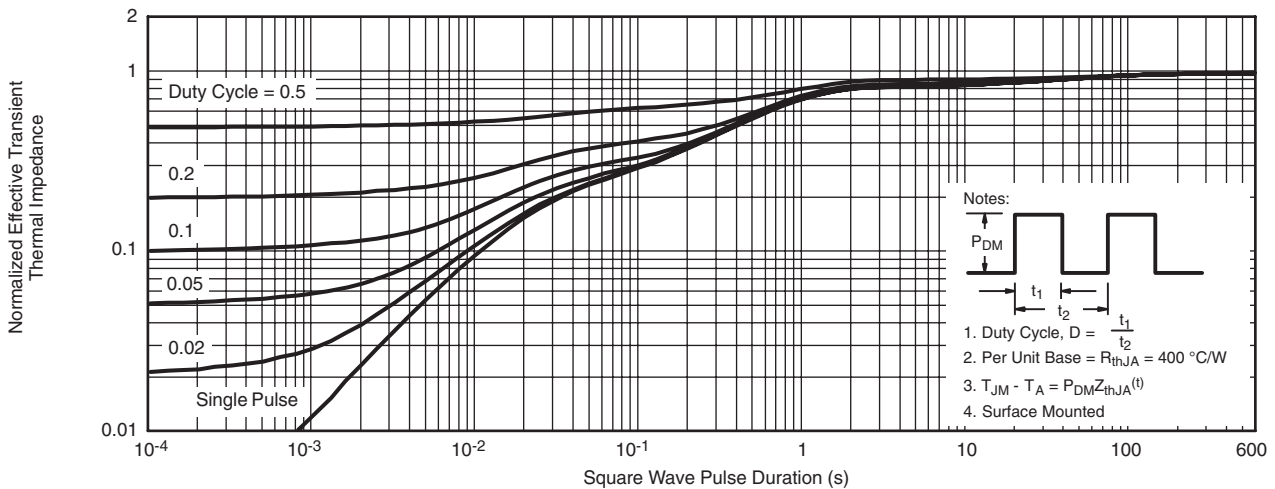
Switching Variation
 R_2 at $V_{IN} = 2.5\text{ V}$, $R_1 = 300\text{ k}\Omega$



Switching Variation
 R_2 at $V_{IN} = 1.8\text{ V}$, $R_1 = 300\text{ k}\Omega$



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

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