



P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

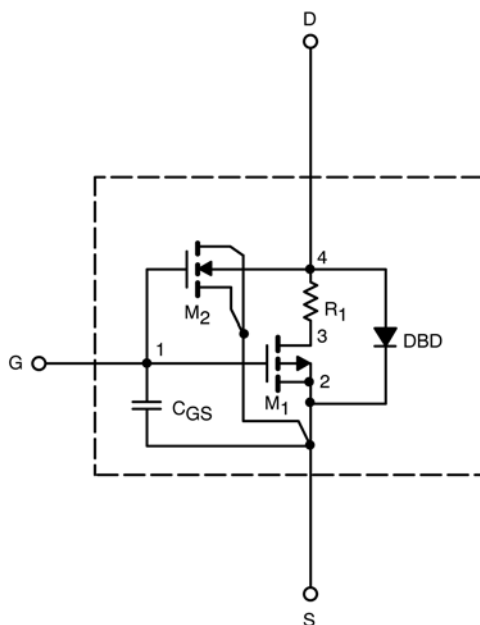
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	2.1		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	73		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -3.2 A	0.061	0.063	Ω
		V _{GS} = -4.5 V, I _D = -2.5 A	0.101	0.105	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -3.2 A	4	5	S
Diode Forward Voltage ^a	V _{SD}	I _S = -0.75 A, V _{GS} = 0 V	-0.76	-0.85	V
Dynamic^b					
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -1.7 A	8	9	nC
Gate-Source Charge	Q _{gs}		1.4	1.4	
Gate-Drain Charge	Q _{gd}		2.4	2.4	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	12	9	ns
Rise Time	t _r		9	12	
Turn-Off Delay Time	t _{d(off)}		29	25	
Fall Time	t _f		9	14	

Notes

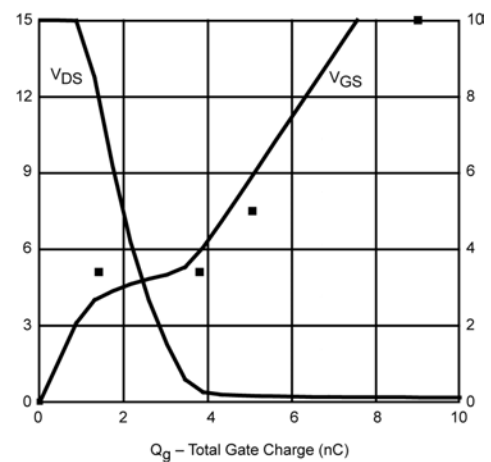
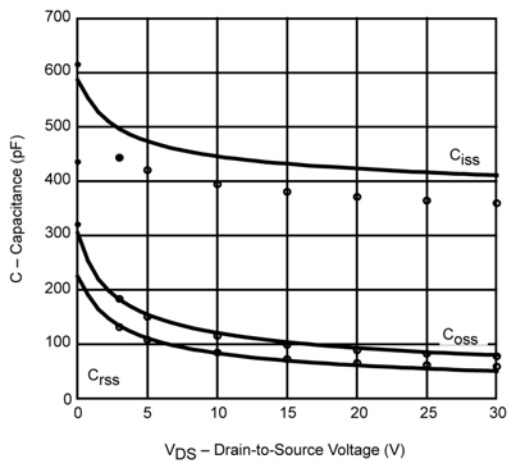
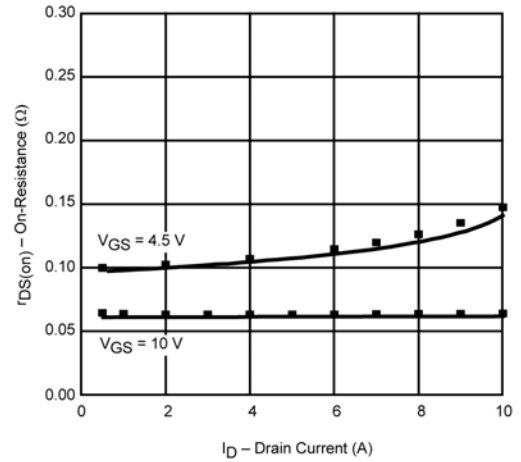
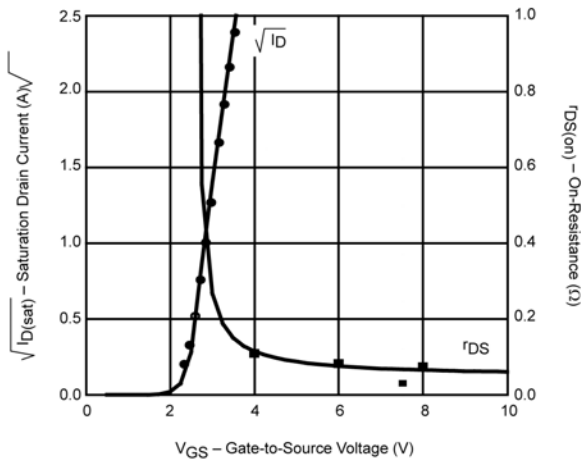
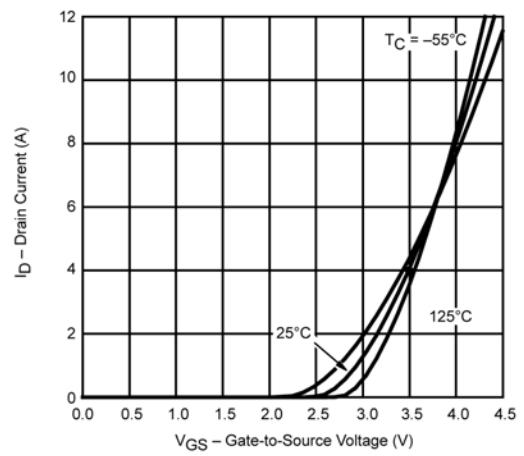
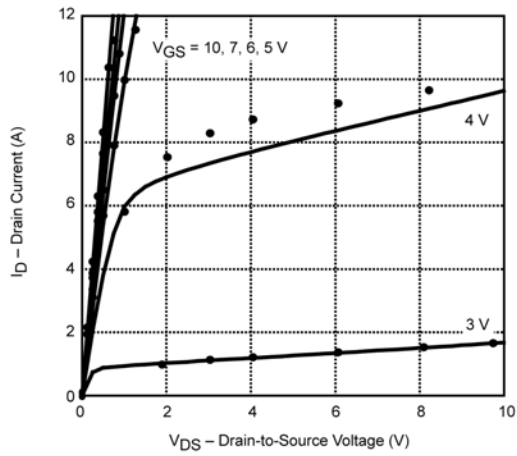
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si2307BDS

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Disclaimer

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