### **SPICE Device Model Si9433BDY**



Vishay Siliconix

## P-Channel 20 V (D-S) MOSFET

#### DESCRIPTION

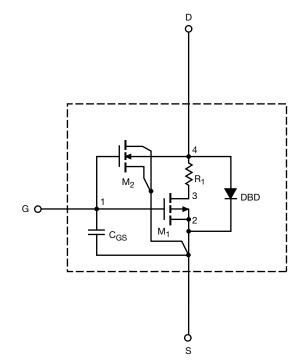
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

### SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$	1.2	-	V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 V, V_{GS} = -4.5 V$	78	-	А
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -6.2 \text{ A}$	0.026	0.030	Ω
		$V_{GS} = -2.7 \text{ V}, \text{ I}_{D} = -5 \text{ A}$	0.043	0.050	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -6.2 \text{ A}$	13	15	S
Diode Forward Voltage	V <sub>SD</sub>	$I_{\rm S}$ = - 2.6 A, $V_{\rm GS}$ = 0 V	- 0.82	- 0.76	V
Dynamic <sup>b</sup>					
Total Gate Charge	Qg	$V_{DS}$ = - 6 V, $V_{GS}$ = - 4.5 V, $I_D$ = - 6.2 A	8	8.8	nC
Gate-Source Charge	Q <sub>gs</sub>		1.8	1.8	
Gate-Drain Charge	Q <sub>gd</sub>		2.4	2.4	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD}$ = - 6 V, R <sub>L</sub> = 6 $\Omega$ I <sub>D</sub> = - 1 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 6 $\Omega$	58	40	ns
Rise Time	t <sub>r</sub>		29	55	
Turn-Off Delay Time	t <sub>d(off)</sub>		58	65	
Fall Time	t <sub>f</sub>		18	30	

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.



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3.0

20

6.0

4.8

3.6

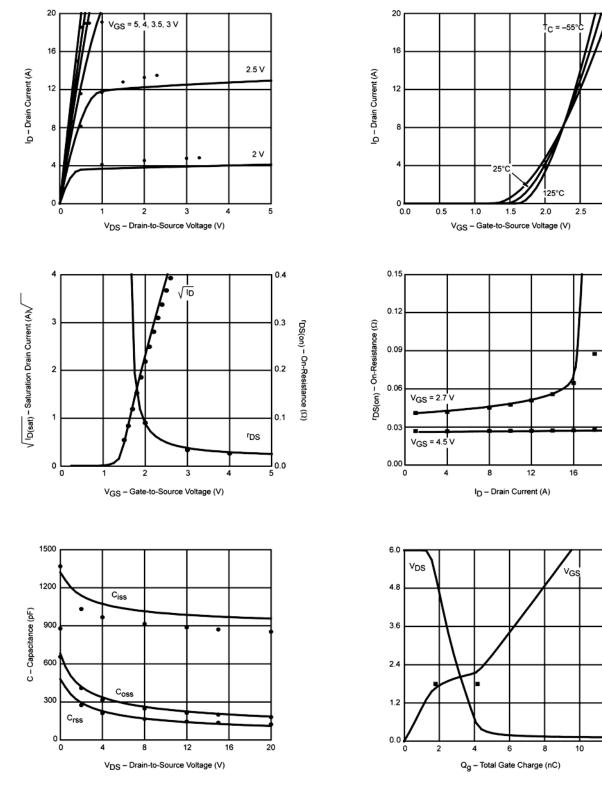
2.4

1.2

0.0

12

### COMPARISON OF MODEL WITH MEASURED DATA (T\_J = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data.

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