



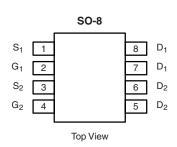
Dual P-Channel 60-V (D-S) 175° MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)			
- 60	$0.120 \text{ at V}_{GS} = -10 \text{ V}$	- 3.1			
	0.150 at V _{GS} = - 4.5 V	- 2.8			

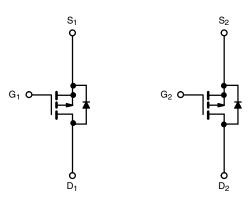
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Compliant to RoHS Directive 2002/95/EC





Ordering Information: Si4948BEY-T1-E3 (Lead (Pb)-free) Si4948BEY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 60		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Dunin Comment /T 450 90\8	T _A = 25 °C	- I _D	- 3.1	- 2.4	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		- 2.6	- 2.0	l
Pulsed Drain Current (10 µs Pulse Width)		I _{DM}	- 25		Α
Continuous Source Current (Diode Conduction) ^a		I _S	- 2	- 1.1	
Avalanche Current	L = 0.1 mH	I _{AS} 15		15]
Single Pulse Avalanche Energy	L = U. I IIII	E _{AS}	11		mJ
Mariana Barra Birating	T _A = 25 °C	D	2.4	2.4 1.4	
Maximum Power Dissipation ^a	T _A = 70 °C	P_{D}	1.7	0.95	W
Operating Junction and Storage Temperature Rar	T _J , T _{stg}	- 55 to 175		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Marrian In action to Austriant	t ≤ 10 s	R	53	62.5	
Maximum Junction-to-Ambient ^a	Steady State	R _{thJA}	85	110	°C/W
Maximum Junction-to-Foot	Steady State	R _{thJF}	30	37	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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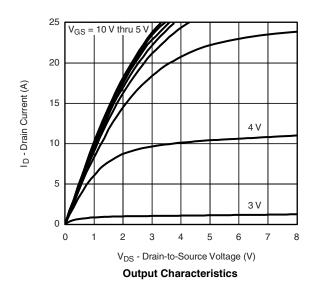
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Vallana Busin Oamant	1	V _{DS} = - 60 V, V _{GS} = 0 V			- 1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 70 °C			- 10	μΑ	
On-State Drain Current ^a	On-State Drain Current ^a		- 25			Α	
D : 0	В	V _{GS} = - 10 V, I _D = - 3.1 A		0.100	0.120	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 0.2 A		0.126	0.150	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 3.1 A		8.5		S	
Diode Forward Voltage ^a	V_{SD}	I _S = - 2 A, V _{GS} = 0 V		- 0.8	- 1.2	V	
Dynamic ^b	•				•		
Total Gate Charge	Q_g			14.5	22		
Gate-Source Charge	Q_{gs}	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -3.1 \text{ A}$		2.2		nC	
Gate-Drain Charge	Q_{gd}			3.7			
Gate Resistance	R_g	f = 1 MHz		14		Ω	
Turn-On Delay Time	t _{d(on)}			10	15		
Rise Time	t _r	V_{DD} = - 30 V, R_L = 30 Ω		15	22		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 6 Ω		50	75	ns	
Fall Time	t _f			35	55		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 2 A, dl/dt = 100 A/μs		30	50		

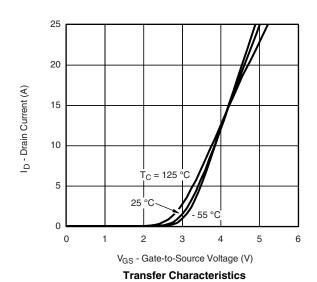
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

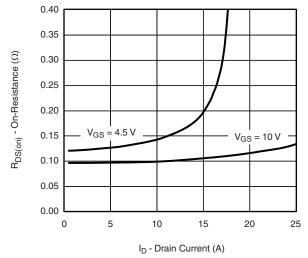




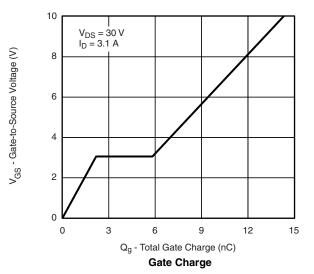


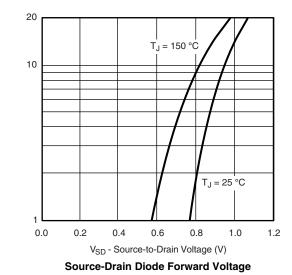


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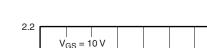
On-Resistance vs. Drain Current

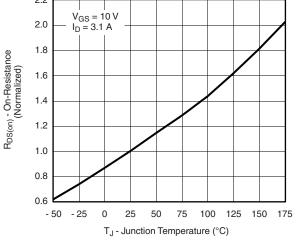




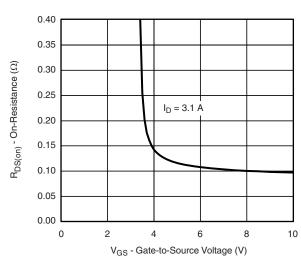
1000 800 C - Capacitance (pF) C_{iss} 600 400 200 Coss Crss 0 10 30 40 50 60 0

V_{DS} - Drain-to-Source Voltage (V) **Capacitance**





On-Resistance vs. Junction Temperature



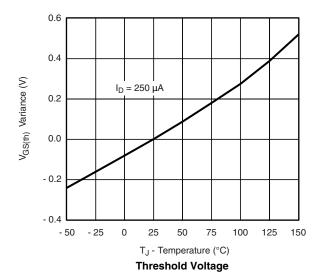
On-Resistance vs. Gate-to-Source Voltage

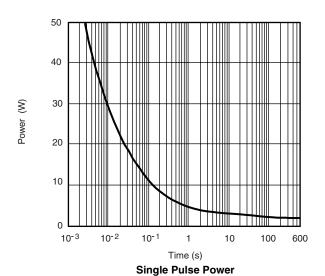
Is - Source Current (A)

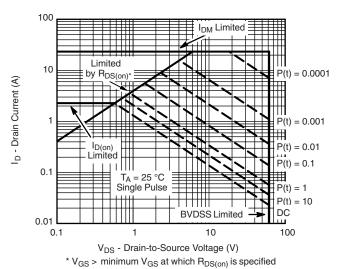
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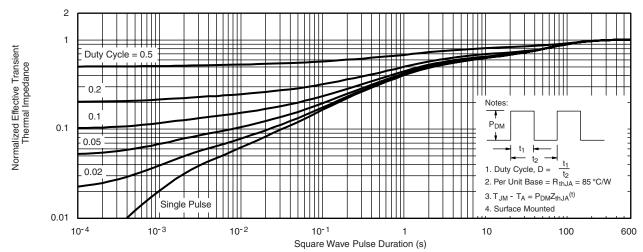
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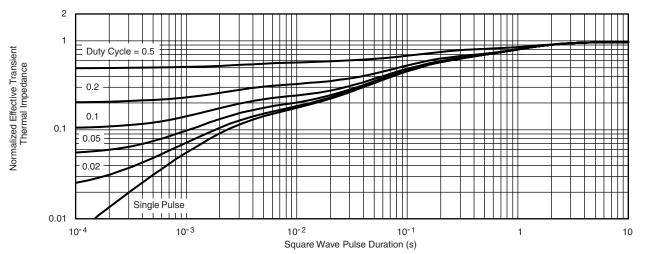
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72847.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Bey 11-Sen-06					

DWG: 5498

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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