DG2131

New Product   **Vishay Siliconix**

Low-Voltage, Sub 1-Ω, Dual SPDT Analog Switch

FEATURES

- Low Voltage Operation
- Low On-Resistance - r_{ON}: 0.57 Ω
- −69 dB OIRR @ 2.7 V, 100 kHz
- ESD Protection >2000 V
- MSOP-10 Package
- Available in Lead (Pb)-Free

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.6-V Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement

DESCRIPTION

The DG2131 is a sub 1-Ω (0.72 Ω @ 2.7 V) dual SPDT analog switch designed for low voltage applications.

The DG2131 has on-resistance matching (less than 0.05 Ω @ 2.7 V) and flatness (less than 0.2 Ω @ 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds makes the DG2131 an ideal interface to low voltage DSP control signals.

The DG2131 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions.

The DG2131 is built on Vishay Siliconix's high-density low voltage CMOS process. An eptiaxial layer is built in to prevent latchup. The DG2131 contains the additional benefit of 2,000-V ESD protection.

Packaged in space saving MSOP-10, the DG2131 is a high performance, low r_{ON} switch for battery powered applications. The DG2131 is available in both standard and lead (Pb)-free packaging. No lead is used in the manufacturing process, for the lead (Pb)-free version, either inside the device/package or on external terminations.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

MSOP-10

V+	1	10 NO2
NO1	2	9 COM2
COM1	3	8 IN2
IN1	4	7 NC2
NC1	5	6 GND

Top View
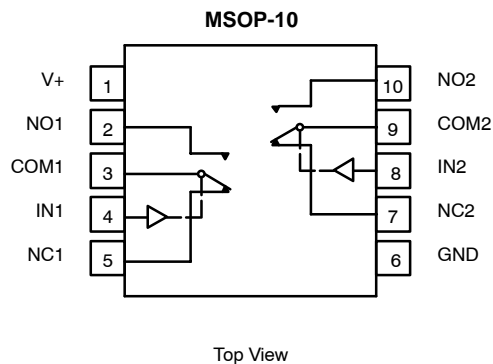
TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Standard Part Number	Lead (Pb)-Free Part Number
-40 to 85°C	MSOP-10 (with Tape and Reel)	DG2131DQ-T1	DG2131DQ-T1—E3

DG2131

Vishay Siliconix   *New Product*

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ . . . . -0.3 to +6 V

IN, COM, NC, NO[a] . . . . -0.3 to (V+ + 0.3 V)

Continuous Current (NO, NC, COM) . . . . ±300 mA

Peak Current . . . . ±500 mA

(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) . . . . -65 to 150°C

ESD per Method 3015.7 . . . . >2 kV

Power Dissipation (Packages)[b]

MSOP-10[c] . . . . 320 mW
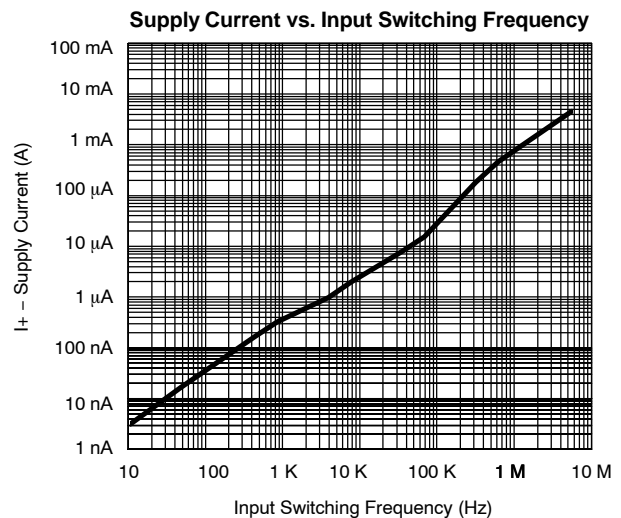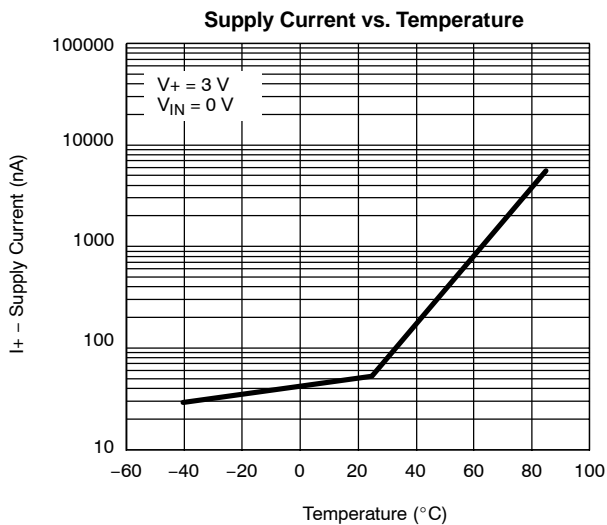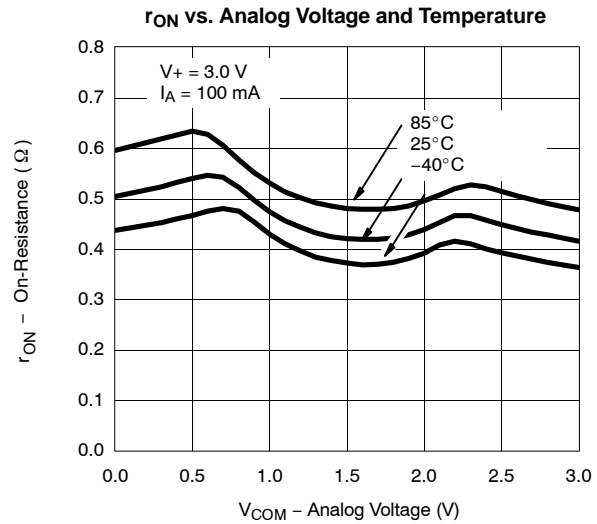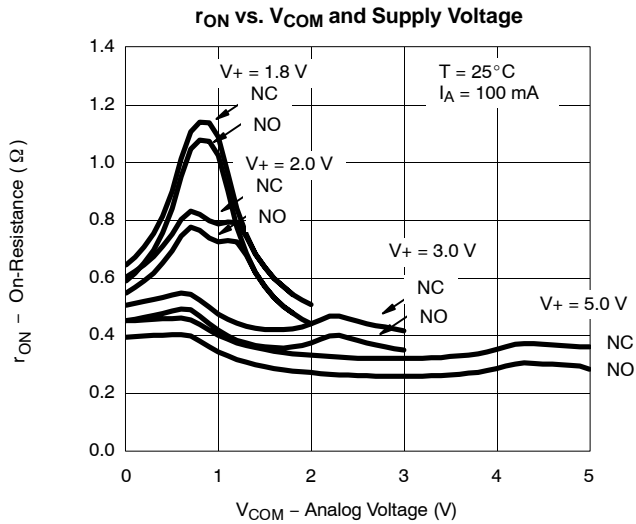
Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 4.0 mW/°C above 70°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
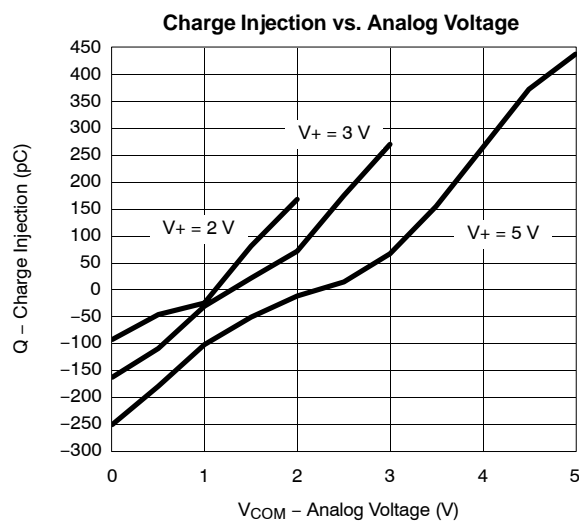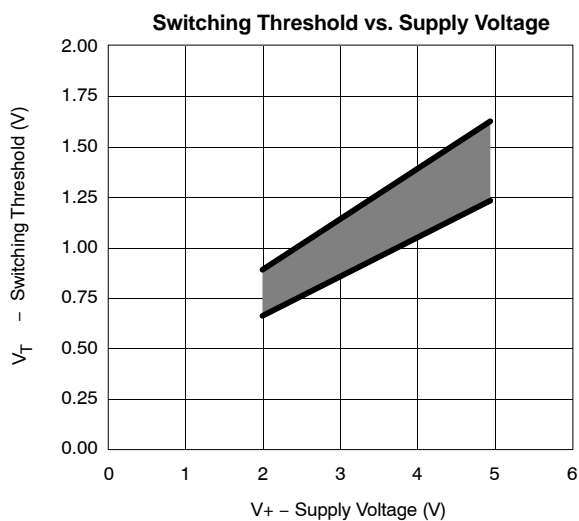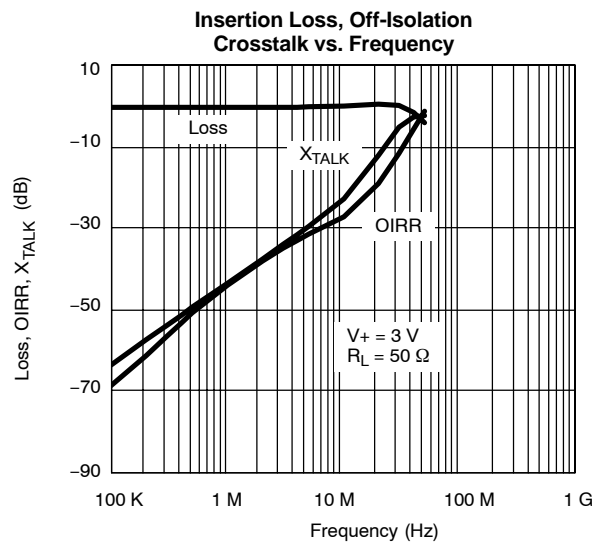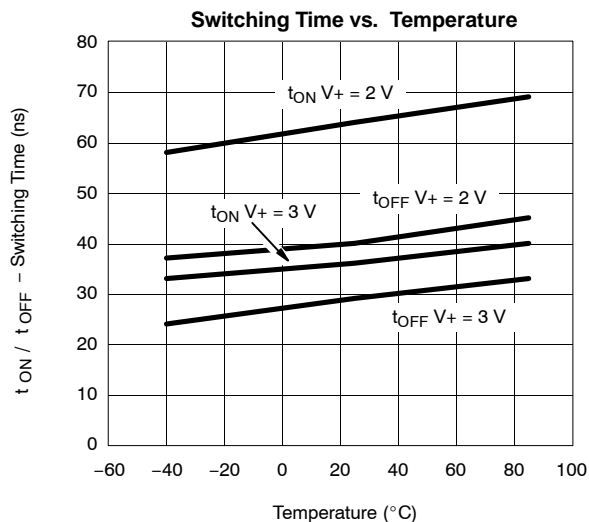
SPECIFICATIONS (V+ = 3 V)

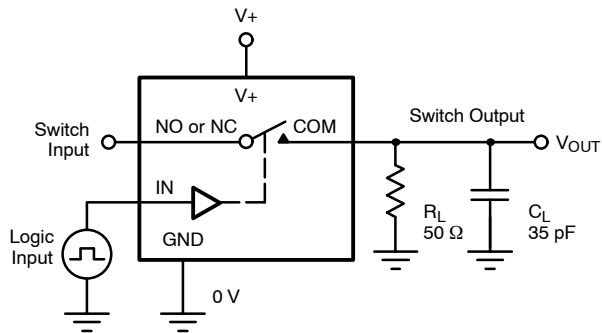| Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.5 or 1.4 V[e]	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.6/1.5 V I_{NO}, I_{NC} = 100 mA	Room Full		0.57	0.75 0.8	Ω
r_{ON} Flatness[d]	r_{ON} Flatness		Room		0.15	0.2	
On-Resistance Match Between Channels[d]	$\Delta r_{DS(on)}$		Room			0.05	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V V_{COM} = 3 V/0.3 V	Room Full	−1 −10		1 10	nA
	$I_{COM(off)}$		Room Full	−1 −10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	−1 −10		1 10	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.4			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF	Room Full		39	69 74	ns
Turn-Off Time	t_{OFF}		Room Full		34	64 68	
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF	Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 1.5 V, R_{GEN} = 0 Ω	Room		20		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 KHz	Room		−69		dB
Crosstalk[d]	X_{TALK}		Room		−64		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		111		pF
	$C_{NC(off)}$		Room		112		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		368		
	$C_{NC(on)}$		Room		368		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1.0	μA

Notes:
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

r_{ON} vs. V_{COM} and Supply Voltage

V+ = 1.8 V
NC
NO
V+ = 2.0 V
NC
NO
T = 25°C
I_A = 100 mA
V+ = 3.0 V
NC
NO
V+ = 5.0 V
NC
NO

r_{ON} – On-Resistance (Ω)

V_{COM} – Analog Voltage (V)

r_{ON} vs. Analog Voltage and Temperature

V+ = 3.0 V
I_A = 100 mA
85°C
25°C
−40°C

r_{ON} – On-Resistance (Ω)

V_{COM} – Analog Voltage (V)

Supply Current vs. Temperature

V+ = 3 V
V_{IN} = 0 V

I+ – Supply Current (nA)

Temperature (°C)

Supply Current vs. Input Switching Frequency

I+ – Supply Current (A)

Input Switching Frequency (Hz)

Leakage Current vs. Temperature

V+ = 3 V
$I_{COM(on)}$
$I_{NO(off)}$, $I_{NC(off)}$
$I_{COM(off)}$

Leakage Current (pA)

Temperature (°C)

Leakage vs. Analog Voltage

V+ = 3 V
$I_{COM(on)}$
$I_{COM(off)}$
$I_{NO(off)}$, $I_{NC(off)}$

Leakage Current (pA)

V_{COM} – Analog Voltage (V)

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Switching Time vs. Temperature

Insertion Loss, Off-Isolation Crosstalk vs. Frequency

Switching Threshold vs. Supply Voltage

Charge Injection vs. Analog Voltage

TEST CIRCUITS

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

C_L (includes fixture and stray capacitance)

FIGURE 1. Switching Time

Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.
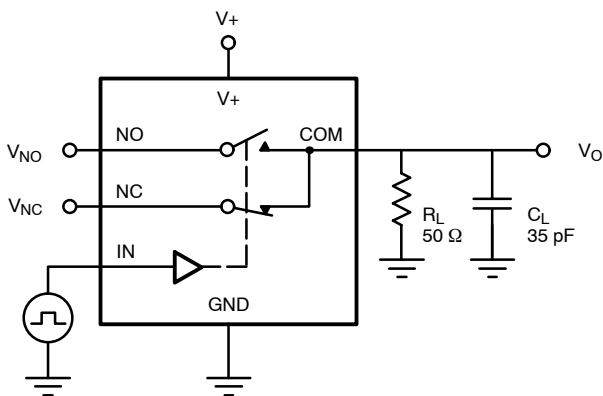
C_L (includes fixture and stray capacitance)
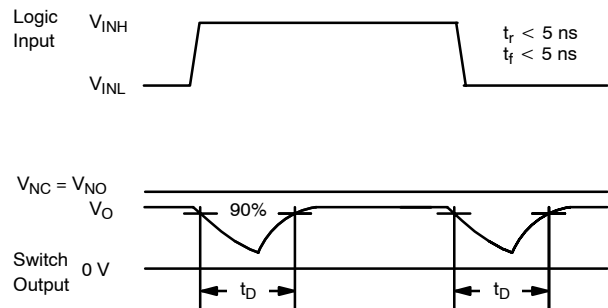
FIGURE 3. Break-Before-Make Interval
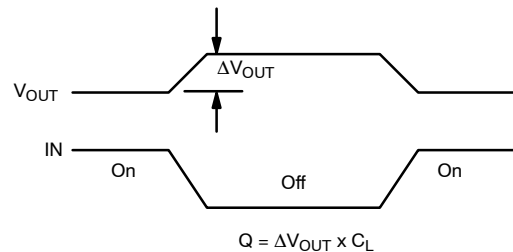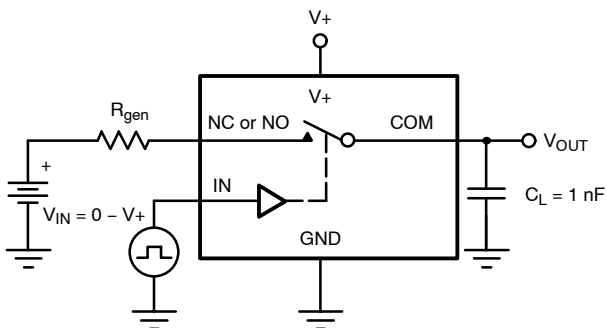

$$Q = \Delta V_{OUT} \times C_L$$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

TEST CIRCUITS

FIGURE 4. Off-Isolation

$$\text{Off Isolation} = 20 \log \frac{V_{COM}}{V_{NO/NC}}$$
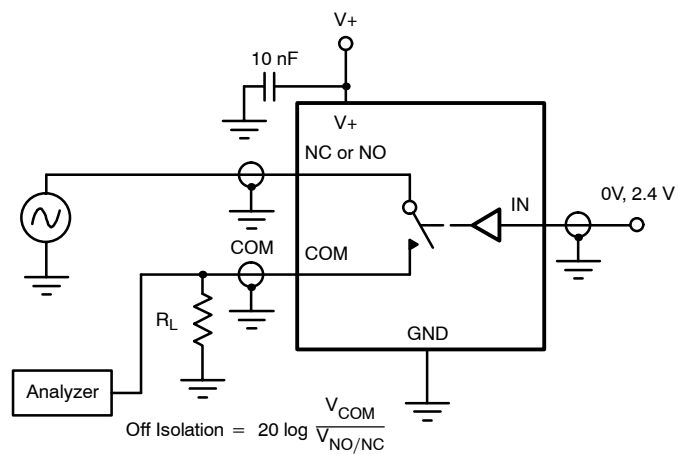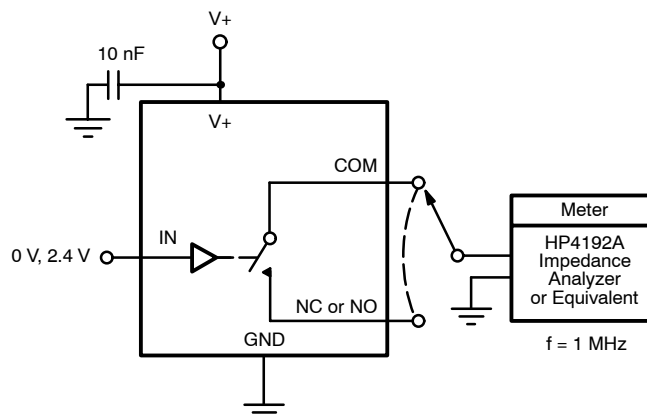

FIGURE 5. Channel Off/On Capacitance

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