Low-Power, High-Speed CMOS Analog Switches

DESCRIPTION

The DG401B, DG403B, DG405B monolithic analog switches are replacements for the popular DG401, DG403, DG405 analog switches and provide improved performance, combining high speed (t_{on}: 100 ns, typ.) with low power consumption make the DG401B series ideal for portable and battery powered applications.

Built on the Vishay Siliconix proprietary high-voltage silicon gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ± 15 V analog range. The DG401B has two independent SPST switches. The DG403B has four SPST switches in NO/NC combinations. The DG405B has four switches in two SPST pairs (see Functional Block Diagrams and Pin Configurations)

The DG401B, DG403B, DG405B is available in both 16-pin plastic dip and 16-pin SOIC packages.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

FEATURES

- 44 V supply max rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 23 Ω
- Low leakage - $I_{D(on)}$: 40 pA
- Fast switching - t_{on}: 100 ns
- Upgrade to DG401B, DG403B, DG405B
- TTL, CMOS compatible
- Single supply capability

APPLICATIONS

- Audio and video switching
- Sample-and-hold circuits
- Test equipment
- PBX, PABX

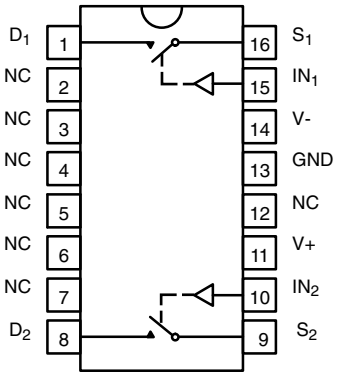
BENEFITS

- Wide dynamic range
- Break-before-make switching action (DG403B only)
- Simple interfacing

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG401B

Dual-In-Line and SOIC



Top View

Two SPST Switches per Package

TRUTH TABLE	
LOGIC	SWITCH
0	Off
1	On

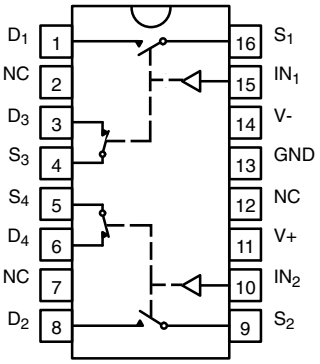
Note

- Logic "0" ≤ 0.8 V
  Logic "1" ≥ 2.4 V

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG403B

Dual-In-Line and SOIC



Top View

Four SPST Switches in Two Pairs per Package

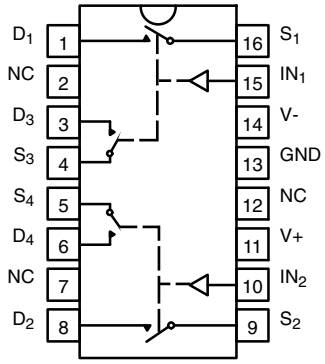
TRUTH TABLE		
LOGIC	**SW1, SW2**	**SW3, SW4**
0	Off	On
1	On	Off

Note

- Logic “0” ≤ 0.8 V
  Logic “1” ≥ 2.4 V

DG405B

Dual-In-Line and SOIC



Top View

Four SPST Switches in Two Pairs per Package

TRUTH TABLE	
LOGIC	**SWITCH**
0	Off
1	On

Note

- Logic “0” ≤ 0.8 V
  Logic “1” ≥ 2.4 V

ORDERING INFORMATION

STANDARD COMMERCIAL PART NUMBER	LEAD (Pb)-FREE COMMERCIAL PART NUMBER	PACKAGE	TEMP. RANGE
DG401BDJ	DG401BDJ-E3	16-pin plastic Dip	-40 °C to +85 °C
DG403BDJ	DG403BDJ-E3		
DG405BDJ	DG405BDJ-E3		
DG401BDY	DG401BDY-E3	16-pin narrow SOIC	
DG403BDY	DG403BDY-E3		
DG405BDY	DG405BDY-E3		
DG401BDY-T1	DG401BDY-T1-E3	16-pin narrow SOIC with tape and reel	
DG403BDY-T1	DG403BDY-T1-E3		
DG405BDY-T1	DG405BDY-T1-E3		

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		LIMIT	UNIT
V+ to V-		44	V
GND to V-		25	
Digital inputs [a], V_S, V_D		(V-) - 0.3 V to (V+) + 0.3 V or 30 mA, whichever occurs first	
Continuous current (any terminal)		30	mA
Peak current, S or D (pulsed at 1 ms, 10 % duty)		100	
Storage temperature	(DJ, DY suffix)	- 65 to +125	°C
Power dissipation (package) [b]	16-pin plastic DIP [c]	450	mW
	16-pin SOIC [d]	600	

Notes

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 6 mW/°C above 75 °C
d. Derate 7.6 mW/°C above 75 °C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

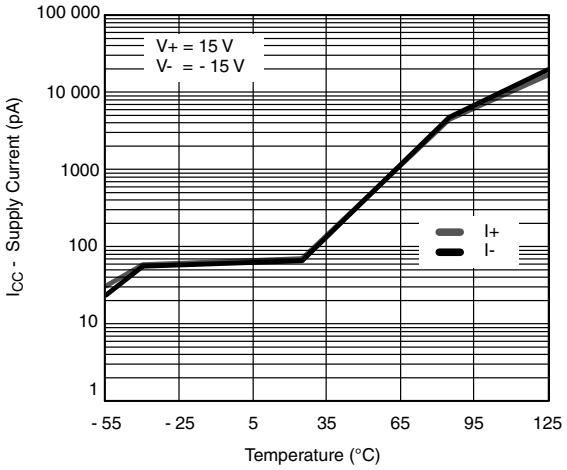
SPECIFICATIONS [a]

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V+ = 15 V, V- = -15 V, V_{IN} = 2.4 V, 0.8 V [f]	TEMP.[b]	D SUFFIX -40 °C TO +85 °C			UNIT
				MIN. [d]	TYP. [c]	MAX. [d]	
Analog Switch							
Analog signal range [e]	V_{ANALOG}		Full	-15	-	15	V
Drain-source on-resistance	$R_{DS(on)}$	I_S = -10 mA, V_D = ± 10 V, V+ = 13.5 V, V- = -13.5 V	Room	-	23	45	Ω
			Full	-	-	55	
Δ drain-source on-resistance	$\Delta R_{DS(on)}$	I_S = -10 mA, V_D = ± 5 V, 0 V, V+ = 16.5 V, V- = -16.5 V	Room	-	0.72	3	
			Full	-	-	5	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V-= -16.5 V, V_D = ± 15.5 V, V_S = ± 15.5 V	Room	-0.5	-0.01	0.5	nA
			Hot	-5	-	5	
	$I_{D(off)}$		Room	-0.5	-0.01	0.5	
			Hot	-5	-	5	
Channel on leakage current	$I_{D(on)}$	V+ = 16.5 V, V-= -16.5 V, V_S = V_D = ± 15.5 V	Room	-1	-0.04	1	
			Hot	-10	-	10	
Digital Control							
Input, high voltage	I_{IL}	V_{IN} under test = 0.8 V, all other = 2.4 V	Full	-1	0.005	1	µA
Input, low voltage	I_{IH}	V_{IN} under test = 2.4 V, all other = 0.8 V	Full	-1	0.005	1	
Dynamic Characteristics							
Turn-on time	t_{on}	R_L = 300 Ω, C_L = 35 pF, see Fig. 2	Room	-	100	150	ns
Turn-off time	t_{off}		Room	-	60	100	
Break-before-make time delay (DG403B)	t_D	R_L = 300 Ω, C_L = 35 pF	Room	5	12	-	
Charge injection	Q	C_L = 10 000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-	60	-	pC
Off isolation reject ratio	OIRR	RL = 100 W, CL = 5 pF, f =1 MHz	Room	-	-81.7	-	dB
Channel-to-channel crosstalk	X_{TALK}		Room	-	-94.8	-	
Source off capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	-	12	-	pF
Drain off capacitance	$C_{D(off)}$		Room	-	12	-	
Channel on capacitance	C_D, $C_{S(on)}$		Room	-	39	-	
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 V or 5 V	Room	-	0.250	0.5	mA
			Full	-	-	1	
Negative Supply Current	I-		Room	-0.5	0.25	-	
			Full	-1	-	-	
Ground current	I_{GND}		Room	-0.5	0.25	-	
			Full	-1	-	-	

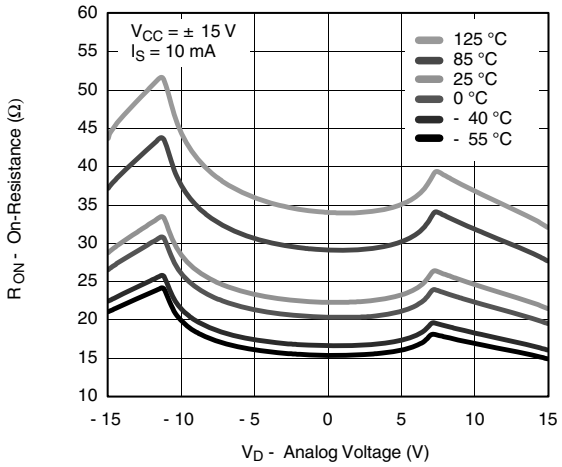
Notes

a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = input voltage to perform proper function

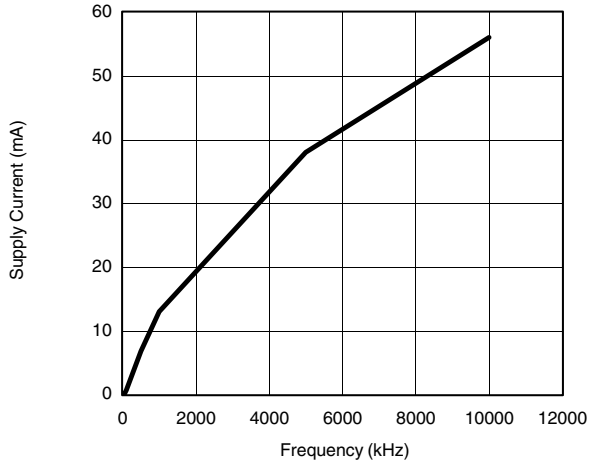
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



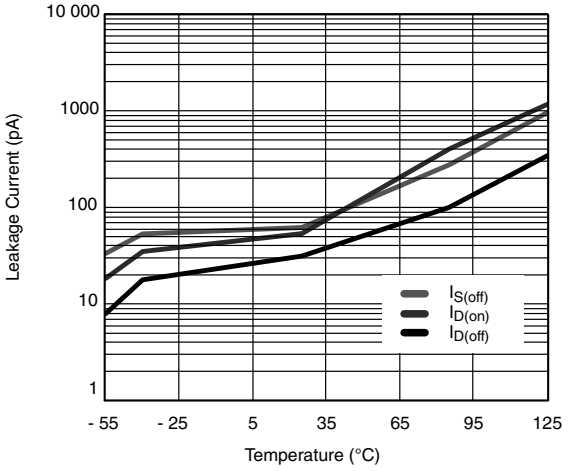
Supply Current vs. Temperature



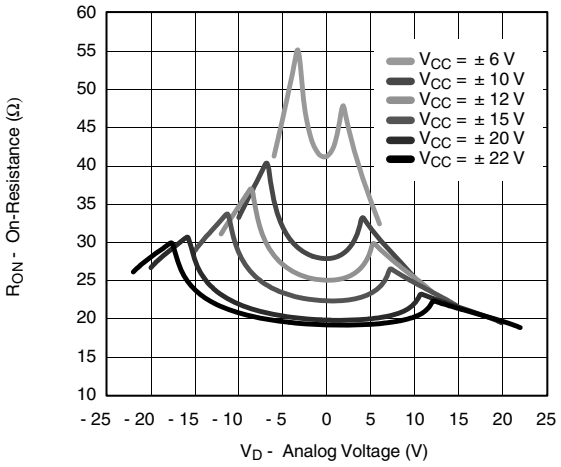
R_{ON} vs. Analog Voltage and Temperature



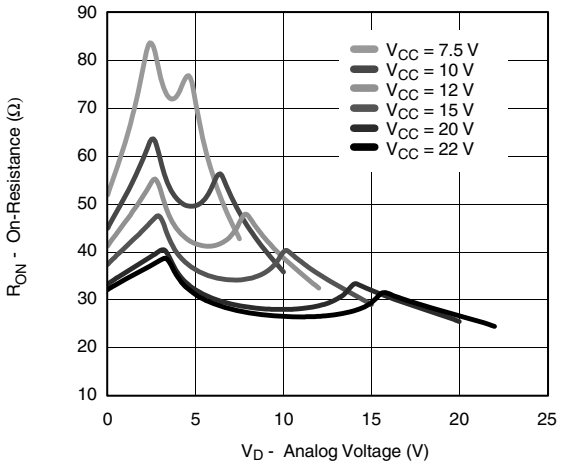
Supply Current vs. Switching Frequency



Leakage Current vs. Temperature

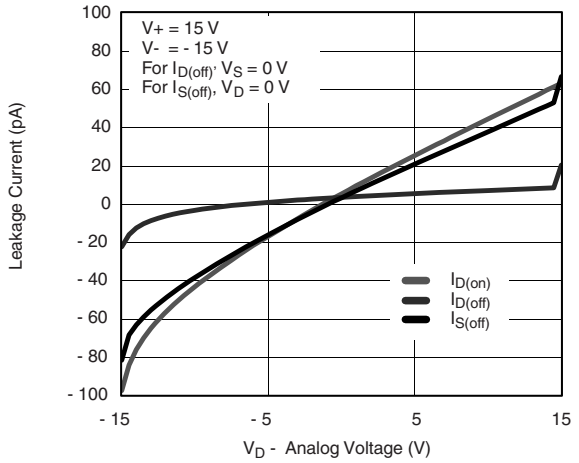


R_{ON} vs. Analog Voltage and Supply Voltage

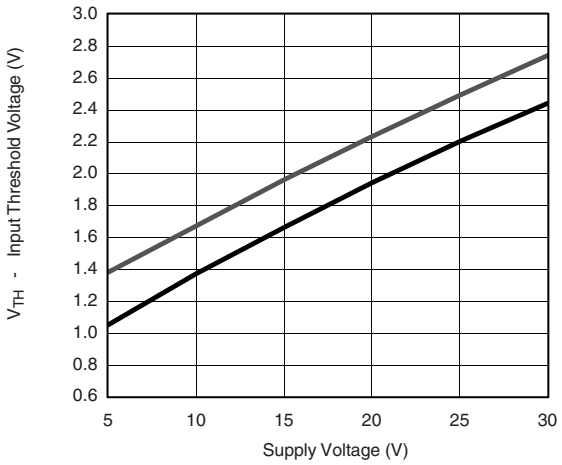


R_{ON} vs. Analog Voltage and Single Supply

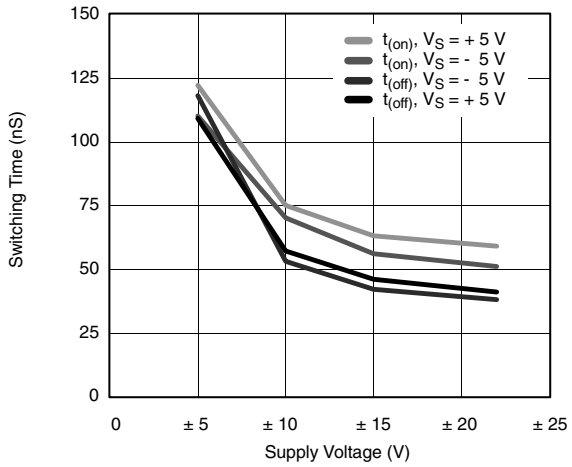
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



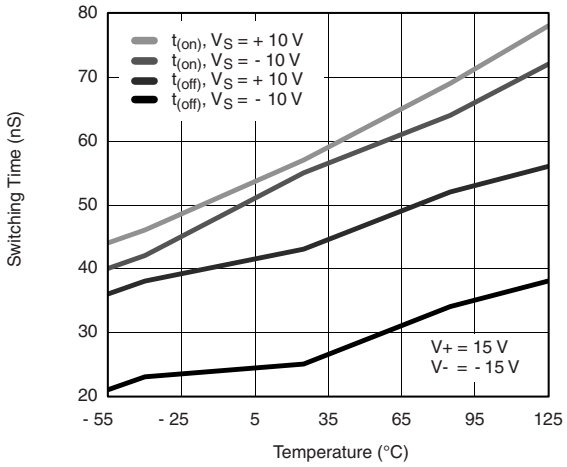
Leakage Current vs. Analog Voltage



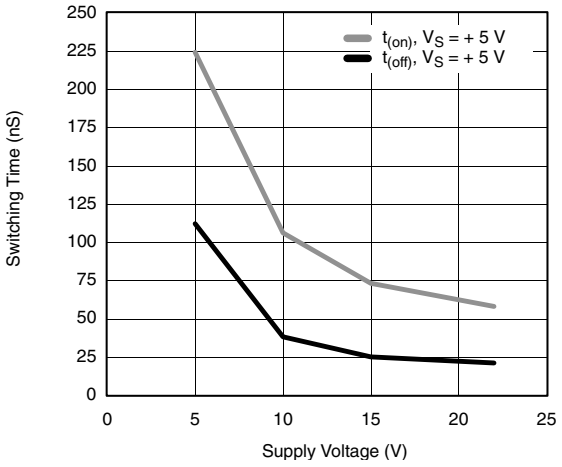
Input Switching Threshold vs. Supply



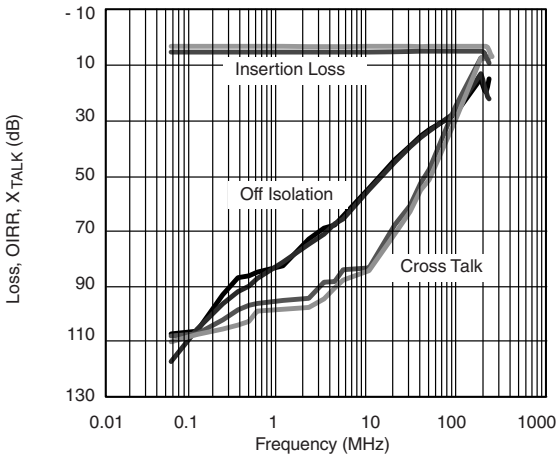
Switching Time vs. Supply Voltage



Switching Time vs. Temperature



Switching Time vs. Single Supply Voltage



Insertion Loss, Off -Isolation Crosstalk vs. Frequency

SCHEMATIC DIAGRAM (typical channel)

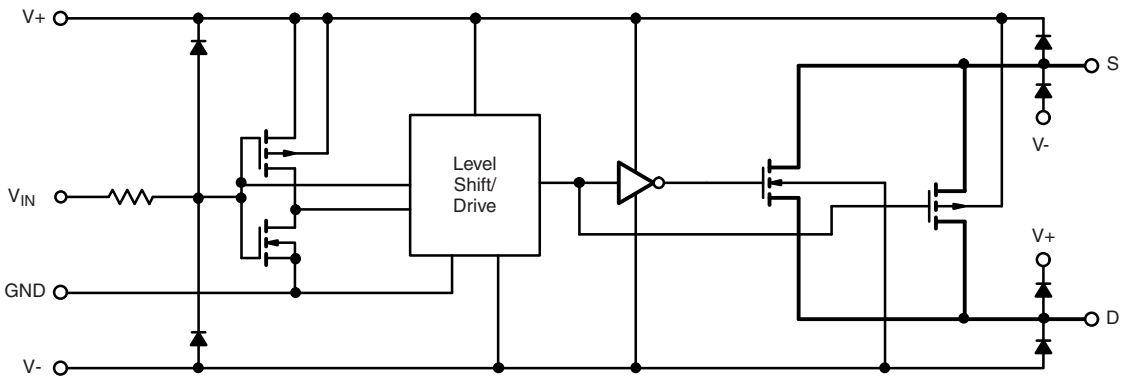
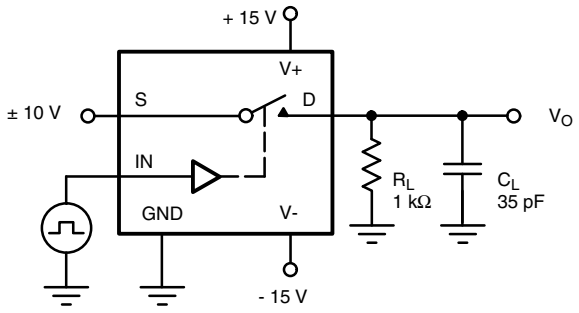


Fig. 1

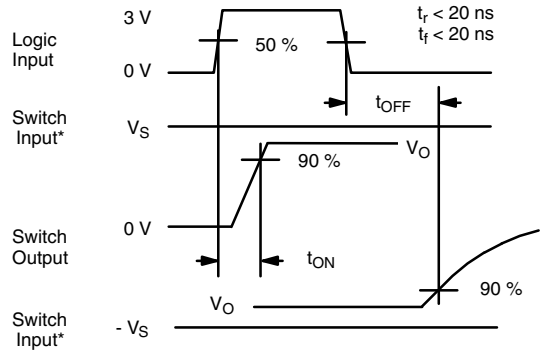
TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

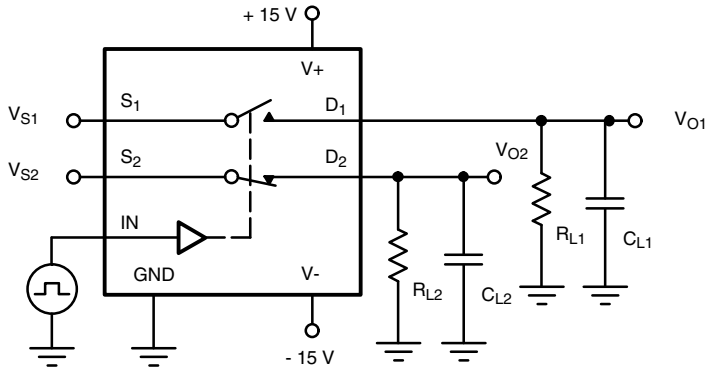
$$V_O = V_S \frac{R_L}{R_L + R_{DS(on)}}$$



* V_S = 10 V for t_{ON}, V_S = - 10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 2 - Switching Time



C_L (includes fixture and stray capacitance)

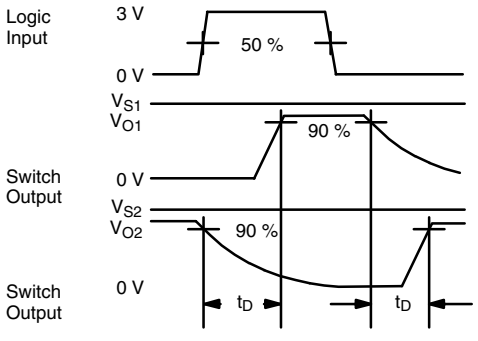
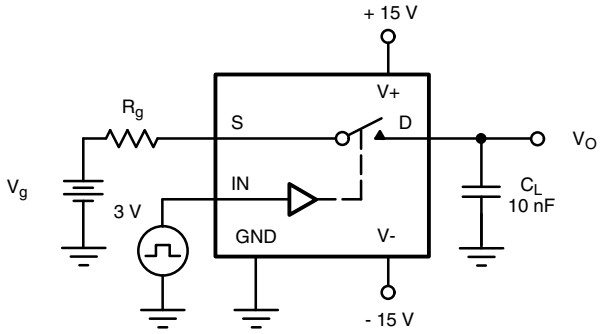


Fig. 3 - Break-Before-Make

TEST CIRCUITS



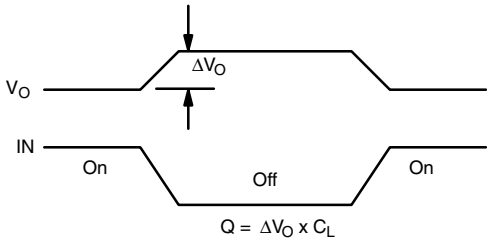


Fig. 4 - Charge Injection

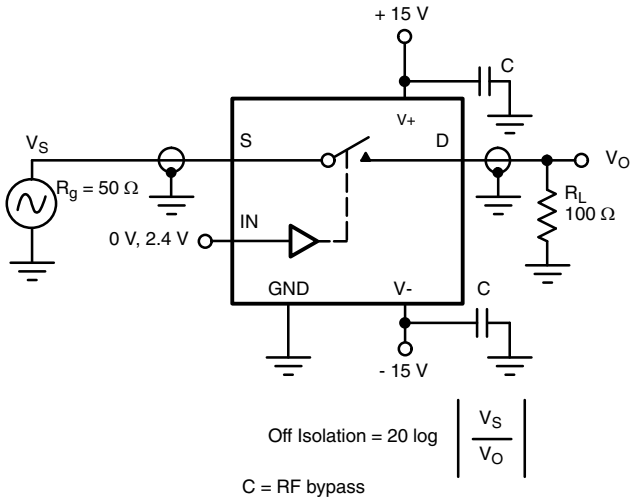


Fig. 5 - Off Isolation

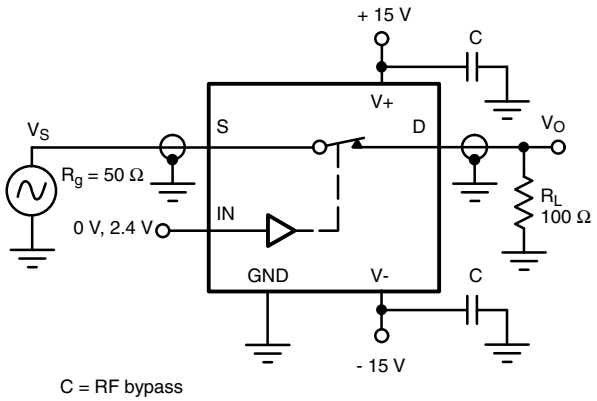


Fig. 7 - Insertion Loss

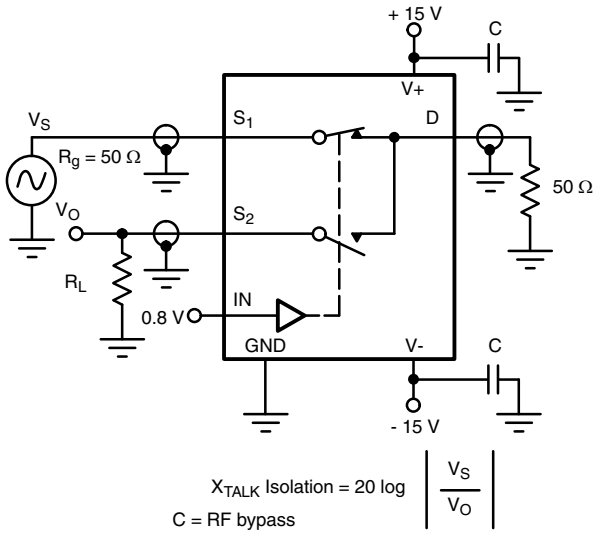


Fig. 6 - Crosstalk

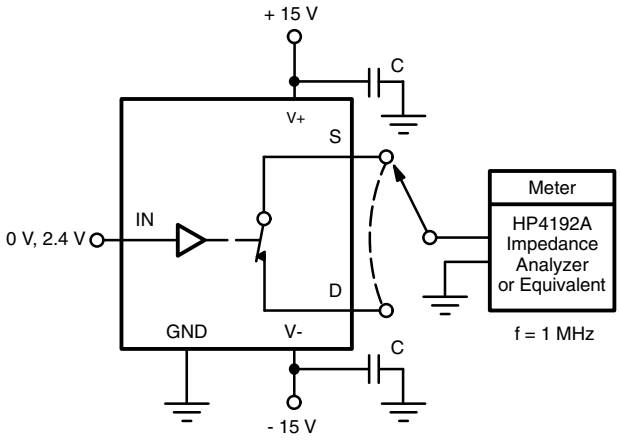


Fig. 8 - Capacitances

APPLICATIONS

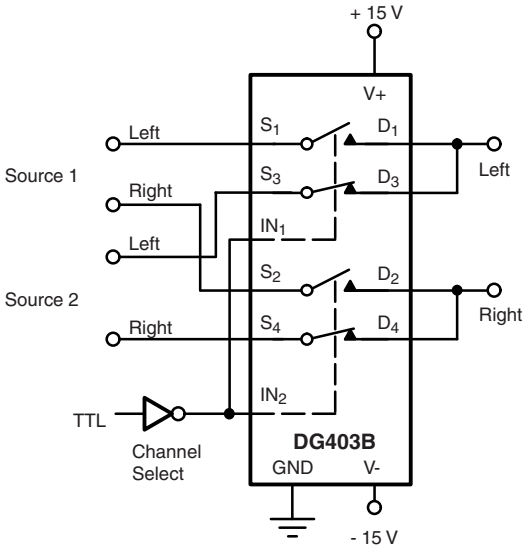


Fig. 9 - Stereo Source Selector

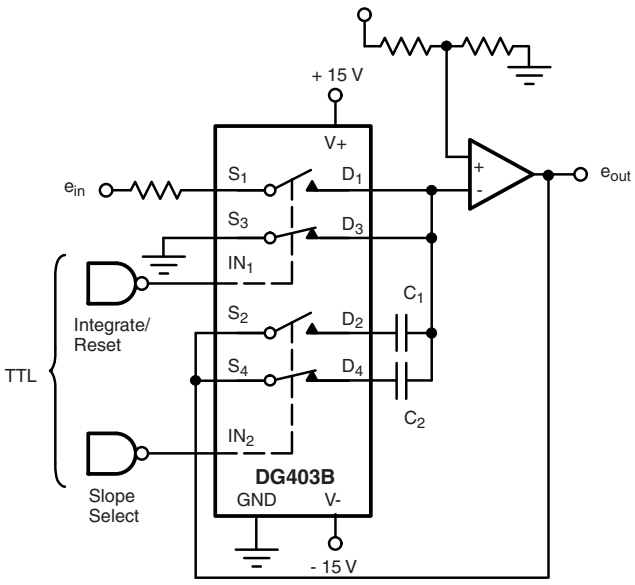


Fig. 10 - Dual Slope Integrator

Dual Slope Integrators

The DG403B is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403B allow for higher clock rates and consequently higher filter operating frequencies.

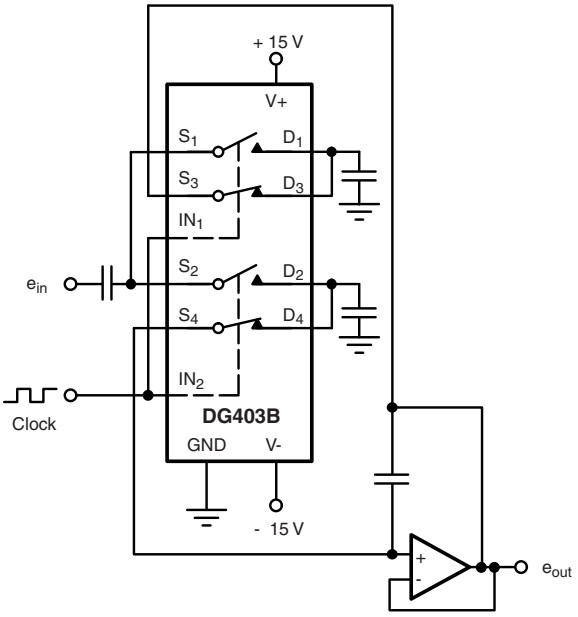


Fig. 11 - Band-Pass Switched Capacitor Filter

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input e_{in}. If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C1 to charge up to the analog input voltage. When e_{in} goes below e_{out} A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

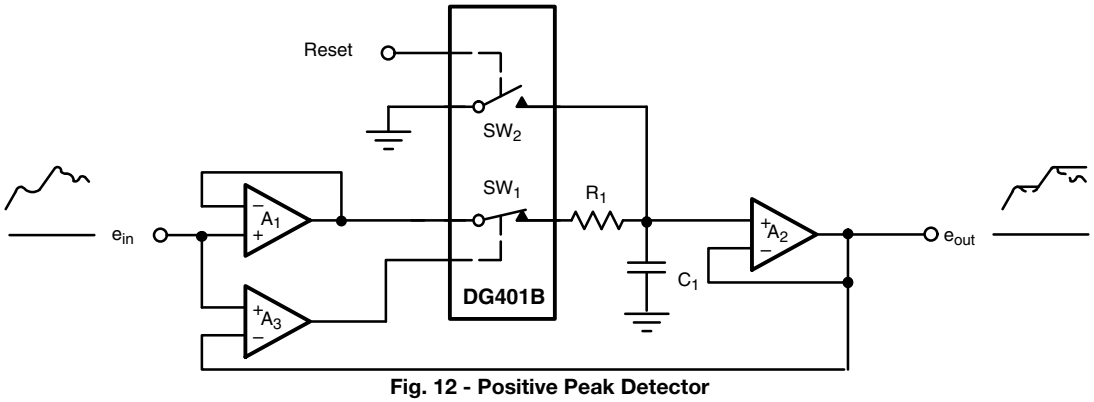


Fig. 12 - Positive Peak Detector

PRODUCT SUMMARY						
Part number	DG401B	DG401B	DG403B	DG403B	DG405B	DG405B
Status code	2	2	2	2	2	2
Configuration	SPST x 2, NO	SPST x 2, NO	SPST x 4, comp, two pairs	SPST x 4, comp, two pairs	SPST x 4, NO, two pairs	SPST x 4, NO, two pairs
Single supply min. (V)	5	5	5	5	5	5
Single supply max. (V)	36	36	36	36	36	36
Dual supply min. (V)	5	5	5	5	5	5
Dual supply max. (V)	22	22	22	22	22	22
On-resistance (Ω)	23	23	23	23	23	23
Charge injection (pC)	60	60	60	60	60	60
Source on capacitance (pF)	39	39	39	39	39	39
Source off capacitance (pF)	12	12	12	12	12	12
Leakage switch on typ. (nA)	0.04	0.04	0.04	0.04	0.04	0.04
Leakage switch off max. (nA)	0.5	0.5	0.5	0.5	0.5	0.5
-3 dB bandwidth (MHz)	-	-	-	-	-	-
Package	Plastic DIP-16	SO-16 (narrow) AS	Plastic DIP-16	SO-16 (narrow) AS	Plastic DIP-16	SO-16 (narrow) AS
Functional circuit / applications	Multi purpose, instrumentation medical and healthcare	Multi purpose, instrumentation medical and healthcare	Multi purpose, instrumentation medical and healthcare	Multi purpose, instrumentation medical and healthcare	Multi purpose, instrumentation medical and healthcare	Multi purpose, instrumentation medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes	Yes	Yes
Turn on time max. (ns)	150	150	150	150	150	150
Crosstalk and off isolation	-94.8	-94.8	-94.8	-94.8	-94.8	-94.8

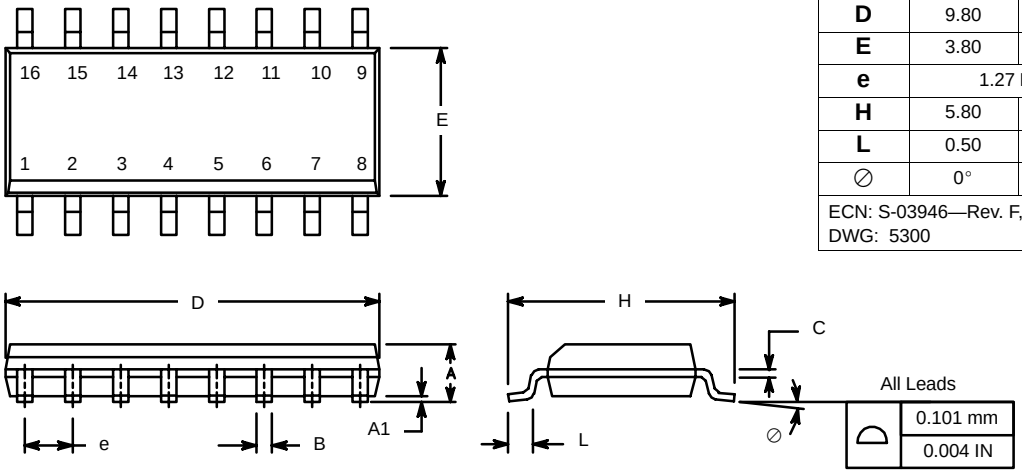
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73069.

SOIC (NARROW): 16-LEAD

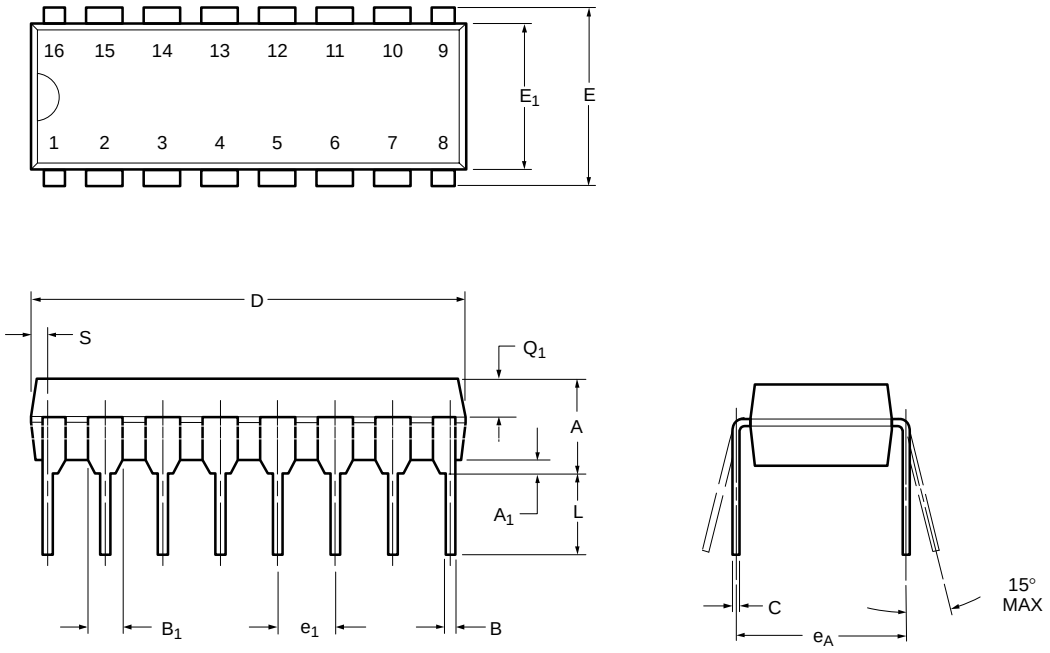
JEDEC Part Number: MS-012

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300

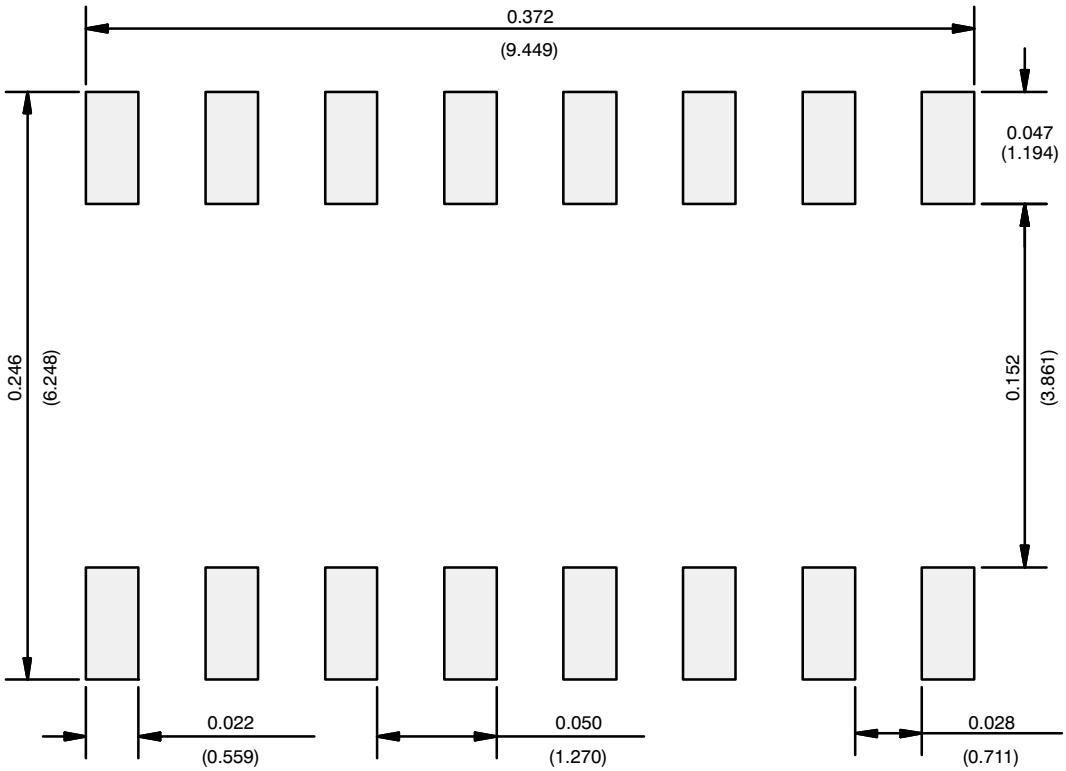


PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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