



### N-Channel 40-V (D-S) Fast Switching MOSFET

#### CHARACTERISTICS

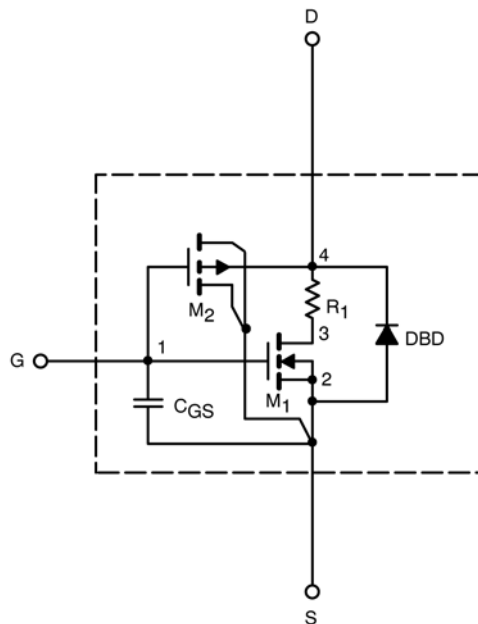
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model Si7116DN



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| SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED) |                     |  |                |               |      |
|---|---------------------|--|----------------|---------------|------|
| Parameter   | Symbol              | Test Condition   | Simulated Data | Measured Data | Unit |
| <b>Static</b>   |                     |  |                |               |      |
| Gate Threshold Voltage  | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA              | 1.8            |               | V    |
| On-State Drain Current <sup>a</sup>                           | I <sub>D(on)</sub>  | V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V                            | 575            |               | A    |
| Drain-Source On-State Resistance <sup>a</sup>                 | r <sub>DS(on)</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 16.4 A                          | 0.0065         | 0.0065        | Ω    |
|   |                     | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14.5 A                         | 0.0084         | 0.0083        |      |
| Forward Transconductance <sup>a</sup>                         | g <sub>fs</sub>     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 16.4 A                          | 60             | 68            | S    |
| Diode Forward Voltage <sup>a</sup>                            | V <sub>SD</sub>     | I <sub>S</sub> = 3.2 A, V <sub>GS</sub> = 0 V                            | 0.80           | 0.80          | V    |
| <b>Dynamic<sup>b</sup></b>                                    |                     |  |                |               |      |
| Total Gate Charge   | Q <sub>g</sub>      | V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 16.4 A | 15             | 15            | nC   |
| Gate-Source Charge  | Q <sub>gs</sub>     |  | 6.7            | 6.7           |      |
| Gate-Drain Charge   | Q <sub>gd</sub>     |  | 5.1            | 5.1           |      |

**Notes**

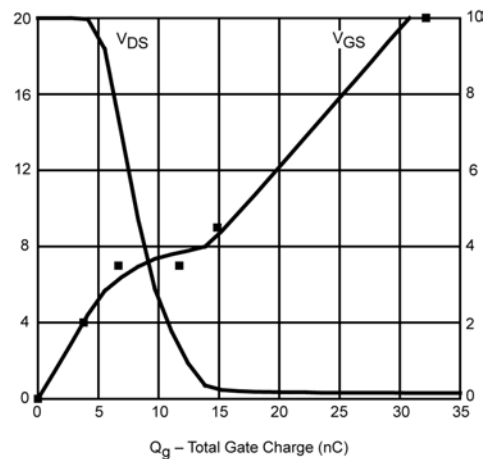
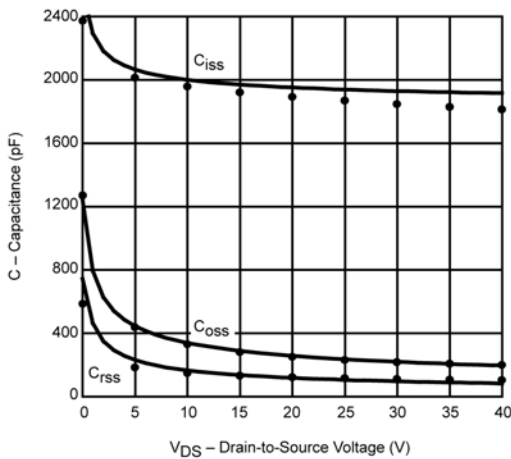
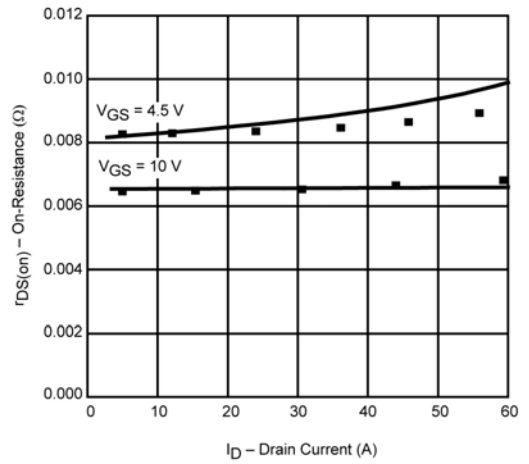
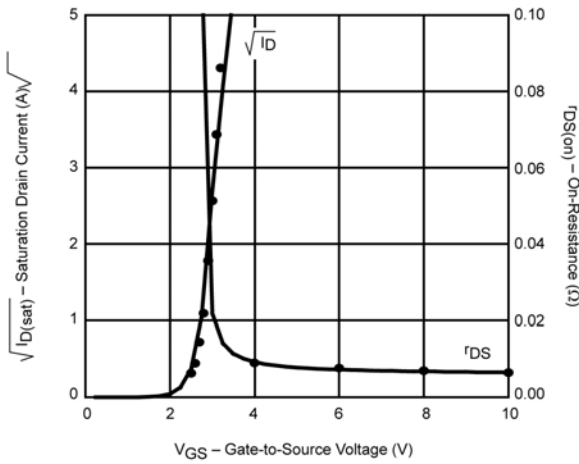
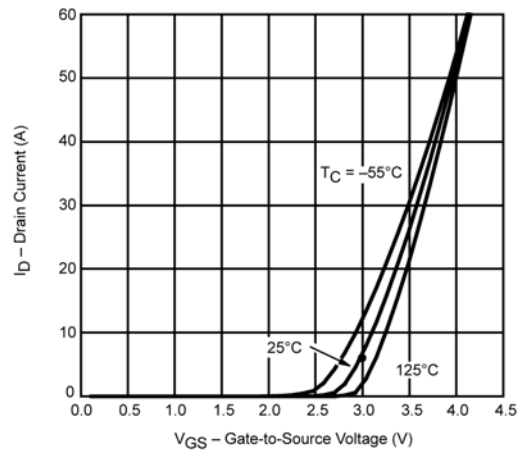
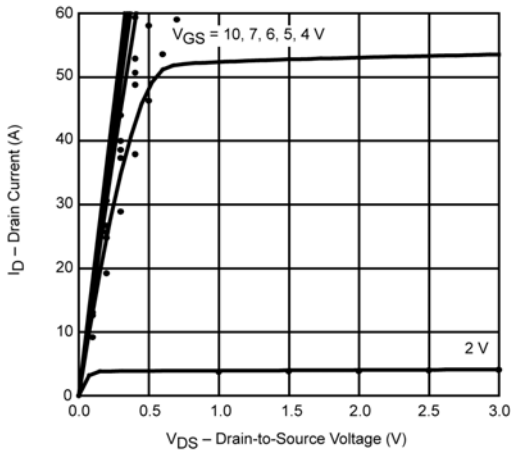
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



## Disclaimer

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