



300 MHz, 2.5 Ω, Dual SPDT Analog Switches

DESCRIPTION

The DG3516, DG3517 are dual SPDT analog switches which operate from 1.8 V to 5.5 V single rail power supply. They are design for audio, video, and USB switching applications.

The devices have 2.5 Ω on-resistance and 300 MHz 3dB bandwidth. 0.2 Ω on-resistance matching and 1 Ω flatness make the device high linearity. The devices are 1.6 V logic compatible within the full operation voltage range.

These switches are built on a sub-micron high density process that brings low power consumption and low voltage performance.

The switches are packaged in MICRO FOOT chip scale package of 4 mm x 3 mm bump array.

As a committed partner to the community and environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For MICRO FOOT analog switch products manufactured with tin/silver/copper (SnAgCu) device termination, the lead (Pb)-free “-E1” suffix is being used as a designator.

FEATURES

- Halogen-free according to IEC 61249-2-21 Definition
- 1.8 V to 5.5 V operation
- 2.5 Ω at 2.7 V R_{ON}
- 300 MHz - 3 dB bandwidth
- ESD method 3015.7 > 2 kV
- Latch-up current 200 mA (JESD 78)
- 1.6 V logic compatible
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

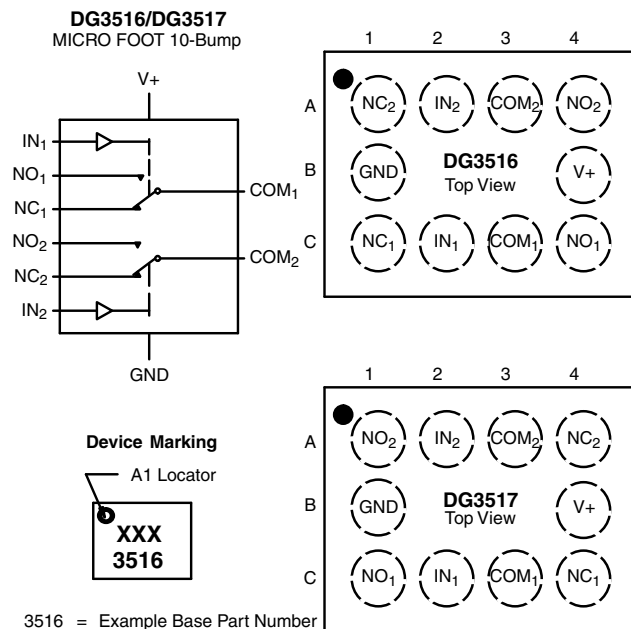
BENEFITS

- Space Saving MICRO FOOT® Package
- High Linearity
- Low Power Consumption
- High Bandwidth
- Full Rail Signal Swing Range

APPLICATIONS

- Cellular Phones
- MP3
- Media Players
- Modems
- Hard Drives
- PCMCIA

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	MICRO FOOT: 10 Bump (4 x 3, 0.5 mm Pitch, 238 μm Bump Height)	DG3516DB-T5-E1 DG3517DB-T5-E1

**ABSOLUTE MAXIMUM RATINGS**

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3)	
Continuous Current (NO, NC, COM)		± 100	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature	(D Suffix)	- 65 to 150	°C
Package Solder Reflow Conditions ^b	IR/Convection	250	
ESD per Method 3015.7		> 2	kV
Power Dissipation (Packages) ^c	MICRO FOOT: 10 Bump (4 mm x 3 mm) ^d	457	mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. Refer to IPC/JEDEC (J-STD-020B).
c. All bumps welded or soldered to PC board.
d. Derate 5.7 mW/°C above 70 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.7 V to 3.6 V, V _{IN} = 0.5 V or 1.4 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit	
				Min. ^b	Typ. ^c	Max. ^b		
Analog Switch								
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V	
On-Resistance ^d	R _{ON}	V+ = 2.7 V I _{NO} , I _{NC} = 10 mA	Room Full		2.5	3.5 3.8	Ω	
R _{ON} Flatness ^d	R _{ON} Flatness		V _{COM} = 1, 1.5, 2 V	Room		0.52		1
On-Resistance Match Between Channels ^d	ΔR _{DS(on)}		V _{COM} = 1.5 V	Room				0.25
Switch Off Leakage Current	I _{NO(off)} I _{NC(off)}	V+ = 3.3 V, V _{NO} , V _{NC} = 0.3 V/3 V, V _{COM} = 3 V/0.3 V	Room Full	- 2 - 20		2 20	nA	
	I _{COM(off)}		Room Full	- 2 - 20		2 20		
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3 V	Room Full	- 2 - 20		2 20		
Digital Control								
Input High Voltage ^d	V _{INH}		Full	1.4			V	
Input Low Voltage	V _{INL}		Full			0.5		
Input Capacitance	C _{in}		Full		5		pF	
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 V or V+	Full	1		1	μA	



SPECIFICATIONS (V ₊ = 3 V)									
Parameter	Symbol	Test Conditions Otherwise Unless Specified V ₊ = 2.7 V to 3.6 V, V _{IN} = 0.5 V or 1.4 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit		
				Min. ^b	Typ. ^c	Max. ^b			
Dynamic Characteristics									
Turn-On Time	t _{ON}	V ₊ = 2.7 V, V _{NO} or V _{NC} = 1.5 V R _L = 300 Ω, C _L = 35 pF	Room Full		21 51 52		ns		
Turn-Off Time	t _{OFF}		Room Full		15 45 46				
Break-Before-Make Time	t _d		Full	1					
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 2 V, R _{GEN} = 0 Ω	Room		1		pC		
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF	f = 1 MHz Room		- 74		dB		
			f = 10 MHz Room		- 54				
Crosstalk ^d	X _{TALK}		f = 1 MHz Room		- 76				
			f = 10 MHz Room		- 56				
N _O , N _C Off Capacitance ^d	C _{NO(off)}	V _{IN} = 0 or V ₊ , f = 1 MHz	Room		12		pF		
	C _{NC(off)}		Room		12				
Channel-On Capacitance ^d	C _{NO(on)}		Room		40				
	C _{NC(on)}		Room		40				
Power Supply									
Power Supply Current	I ₊		V _{IN} = 0 V or V ₊	Room Full				1 1	μA

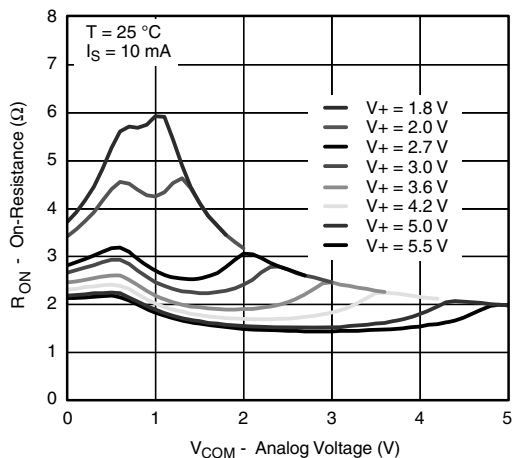
SPECIFICATIONS ($V_+ = 5\text{ V}$)									
Parameter	Symbol	Test Conditions Otherwise Unless Specified $V_+ = 4.2\text{ V}$ to 5.5 V , $V_{IN} = 0.8\text{ V}$ or 2 V^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit		
				Min. ^b	Typ. ^c	Max. ^b			
Analog Switch									
Analog Signal Range ^d	V_{NO}, V_{NC}, V_{COM}		Full	0		V_+	V		
On-Resistance ^d	R_{ON}	$V_+ = 4.2\text{ V}$ $I_{NO}, I_{NC} = 10\text{ mA}$	Room Full		2.2	2.9 3.1	Ω		
R_{ON} Flatness ^d	R_{ON} Flatness		Room		0.53	1			
On-Resistance Match Between Channels ^d	$\Delta R_{DS(on)}$		Room			0.25			
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	$V_+ = 5.5\text{ V}$, $V_{NO}, V_{NC} = 1\text{ V}/4.5\text{ V}$, $V_{COM} = 4.5\text{ V}/1\text{ V}$	Room Full	- 2 - 20		2 20	nA		
	$I_{COM(off)}$		Room Full	- 2 - 20		2 20			
Channel-On Leakage Current	$I_{COM(on)}$	$V_+ = 5.5\text{ V}$, $V_{NO}, V_{NC} = V_{COM} = 1\text{ V}/4.5\text{ V}$	Room Full	- 2 - 20		2 20			
Digital Control									
Input High Voltage ^d	V_{INH}		Full	2			V		
Input Low Voltage	V_{INL}		Full			0.8			
Input Capacitance	C_{in}		Full		5		pF		
Input Current	I_{INL} or I_{INH}	$V_{IN} = 0$ or V_+	Full	1		1	μA		
Dynamic Characteristics									
Turn-On Time	t_{ON}	$V_+ = 4.2\text{ V}$, V_{NO} or $V_{NC} = 3\text{ V}$ $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$	Room Full		15	45 46	ns		
Turn-Off Time	t_{OFF}		Room Full		12	42 43			
Break-Before-Make Time	t_d		Full	1					
Charge Injection ^d	Q_{INJ}	$C_L = 1\text{ nF}$, $V_{GEN} = 2\text{ V}$, $R_{GEN} = 0\ \Omega$	Room		1		pC		
Off-Isolation ^d	OIRR	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$	Room		- 74		dB		
Crosstalk ^d	X_{TALK}		f = 1 MHz	Room		- 54			
			f = 10 MHz	Room		- 78			
			f = 10 MHz	Room		- 56			
N_O, N_C Off Capacitance ^d	$C_{NO(off)}$	$V_{IN} = 0$ or V_+ , f = 1 MHz	Room		12		pF		
	$C_{NC(off)}$		Room		12				
Channel-On Capacitance ^d	$C_{NO(on)}$		Room		40				
	$C_{NC(on)}$		Room		40				
Power Supply									
Power Supply Current	I_+		$V_{IN} = 0\text{ V}$ or V_+	Room Full				1 1	μA

Notes:

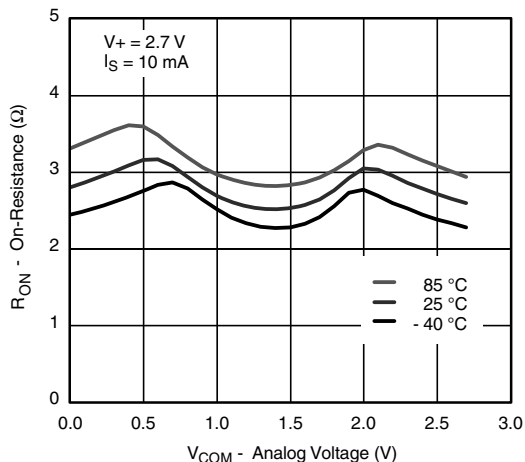
- Room = 25 °C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5 V testing, not production tested.



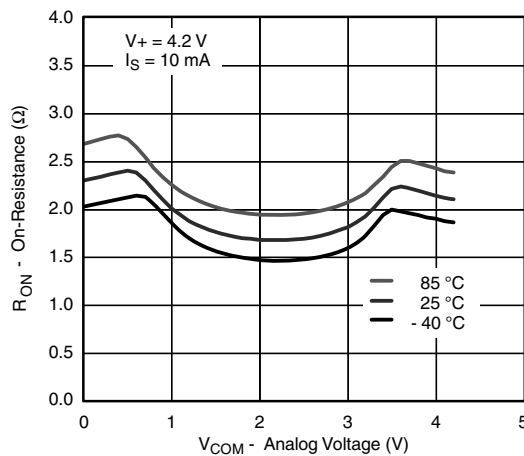
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



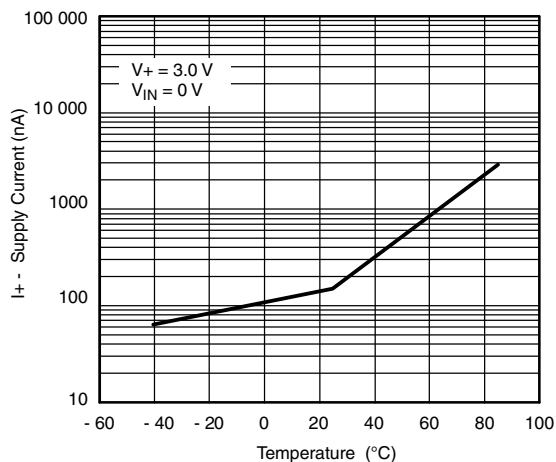
RON vs. VCOM and Single Supply Voltage



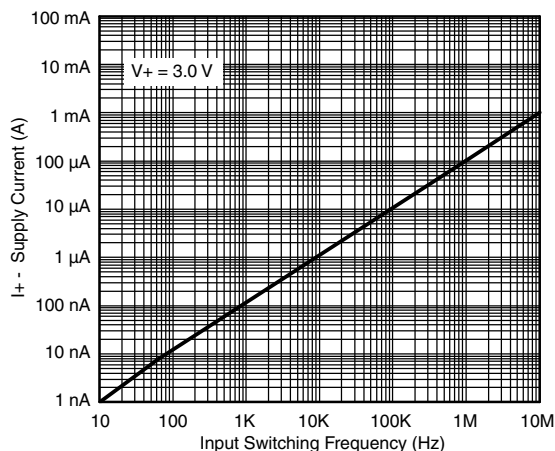
RON vs. Analog Voltage and Temperature



RON vs. Analog Voltage and Temperature



Supply Current vs. Temperature



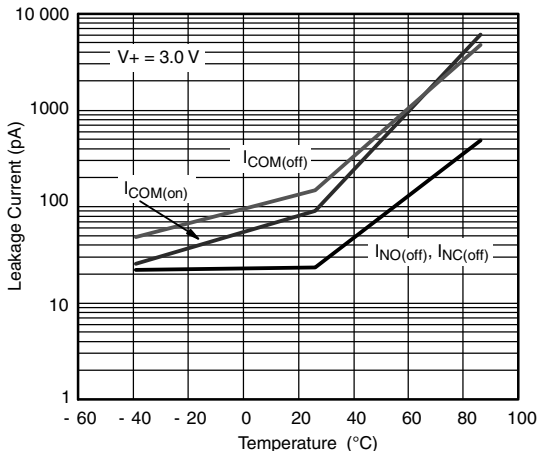
Supply Current vs. Input Switching Frequency

DG3516, DG3517

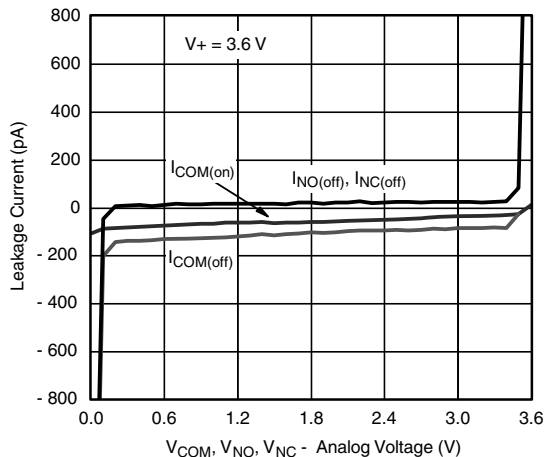


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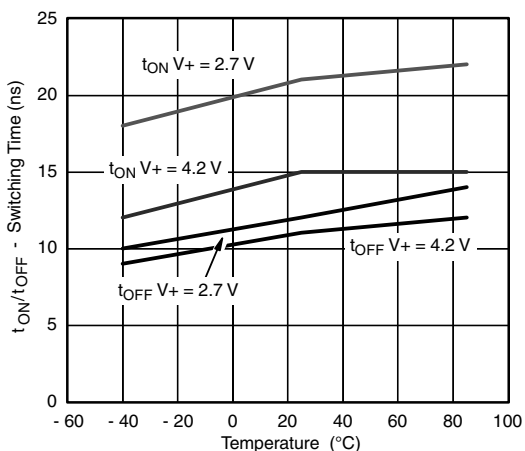
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



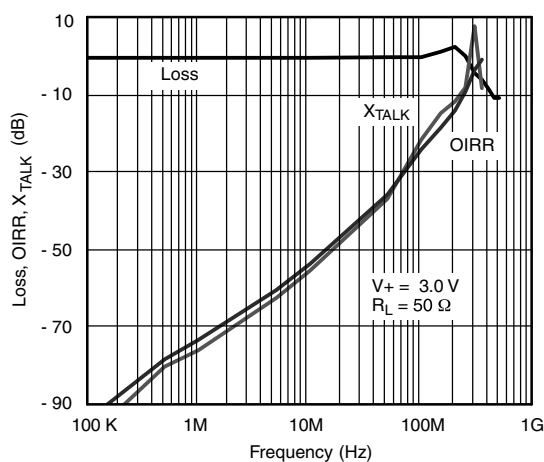
Leakage Current vs. Temperature



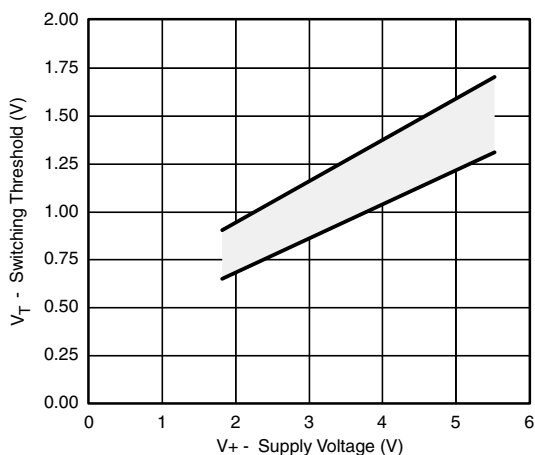
Leakage vs. Analog Voltage



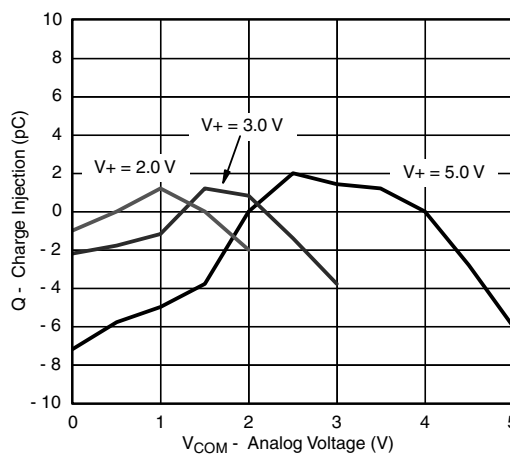
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency



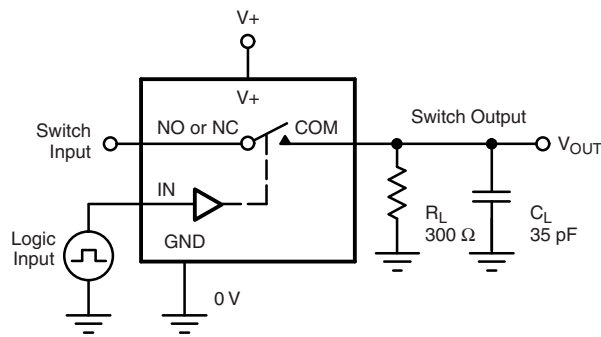
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

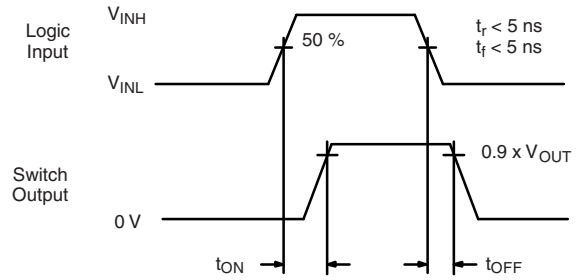


TEST CIRCUITS



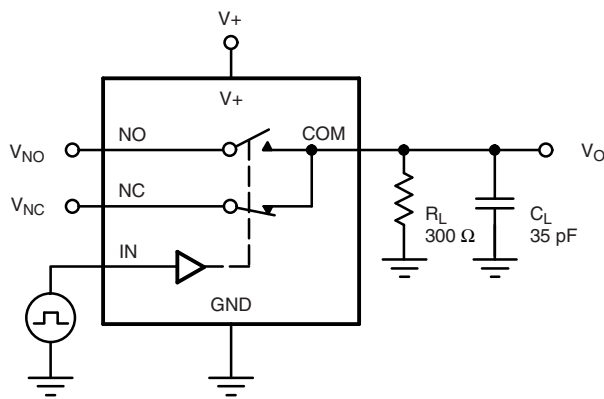
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

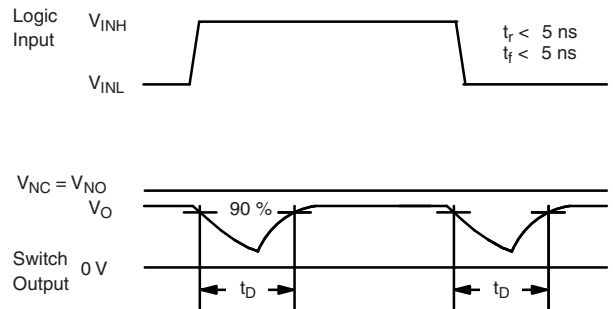
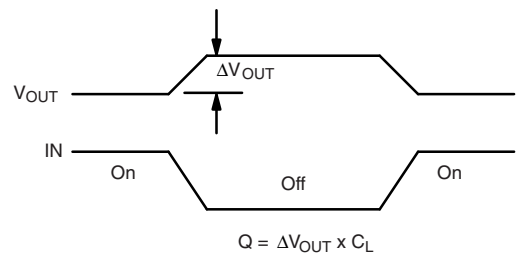
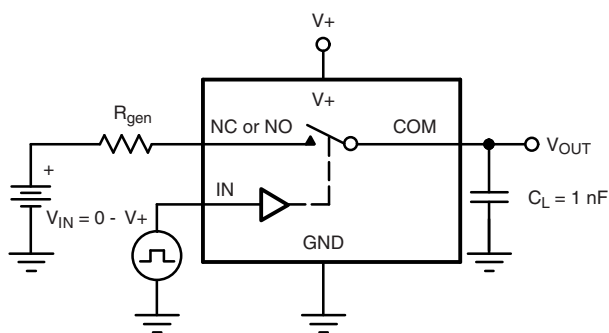


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

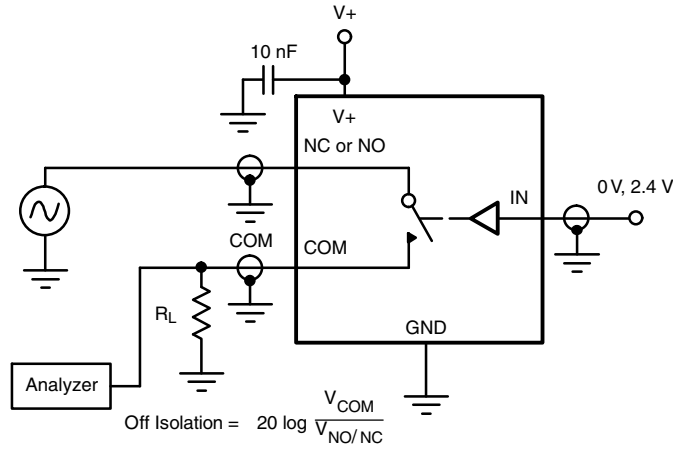


Figure 4. Off-Isolation

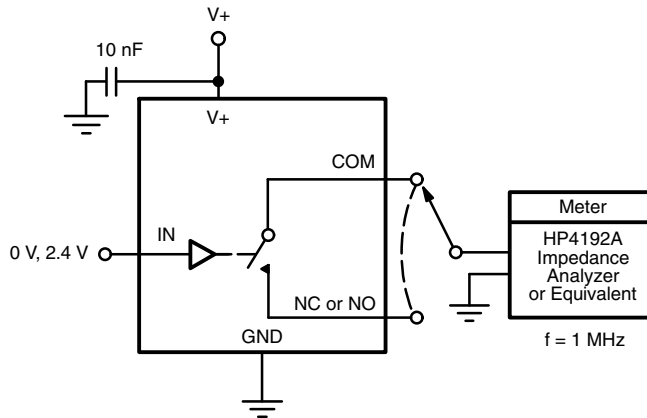
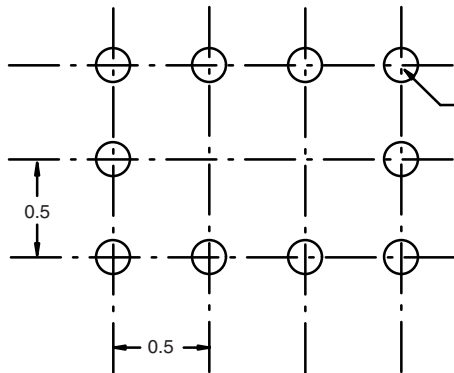


Figure 5. Channel Off/On Capacitance



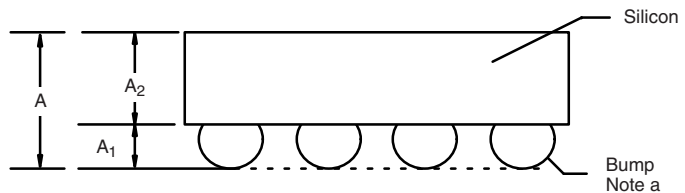
PACKAGE OUTLINE

MICRO FOOT: 10 BUMP (4 x 3 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)

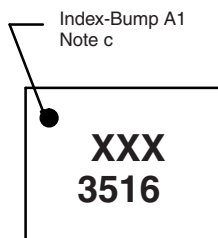


Recommended Land Pattern

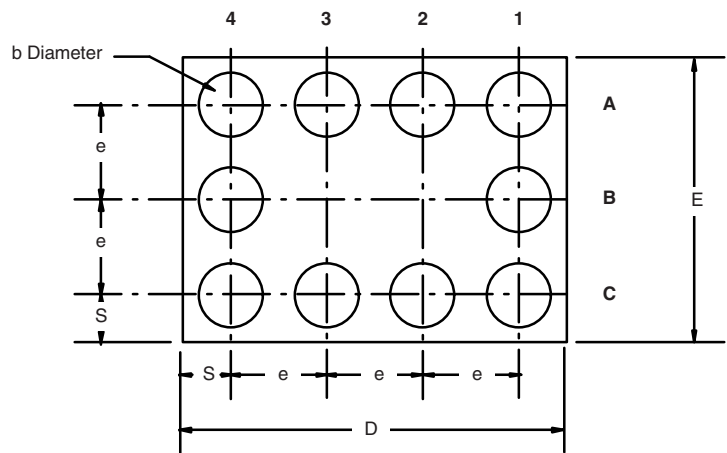
10 x \varnothing 0.150 ~ 0.229
 Note b
 Solder Mask \varnothing ~ Pad Diameter + 0.1



Bump
 Note a



Top Side (Die Back)



Notes (Unless Otherwise Specified):

- a. Bump is Lead (Pb)-free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser Mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

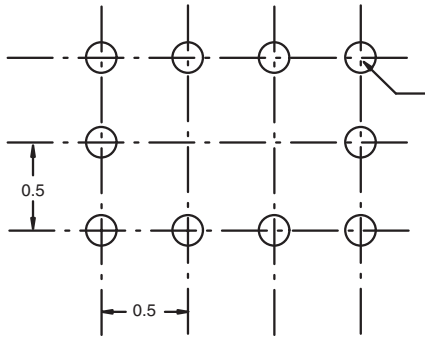
Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.688	0.753	0.0271	0.0296
A ₁	0.218	0.258	0.0086	0.0102
A ₂	0.470	0.495	0.0185	0.0195
b	0.306	0.346	0.0120	0.0136
D	1.980	2.020	0.0780	0.0795
E	1.480	1.520	0.0583	0.0598
e	0.5 BASIC		0.0197 BASIC	
S	0.230	0.270	0.0091	0.0106

Notes:

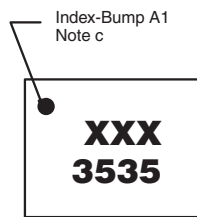
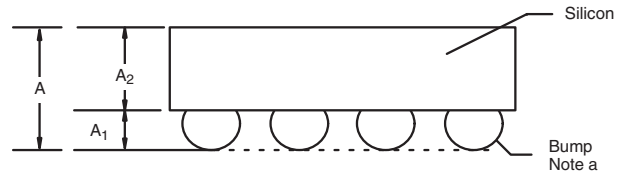
- a. Use millimeters as the primary measurement.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73404.

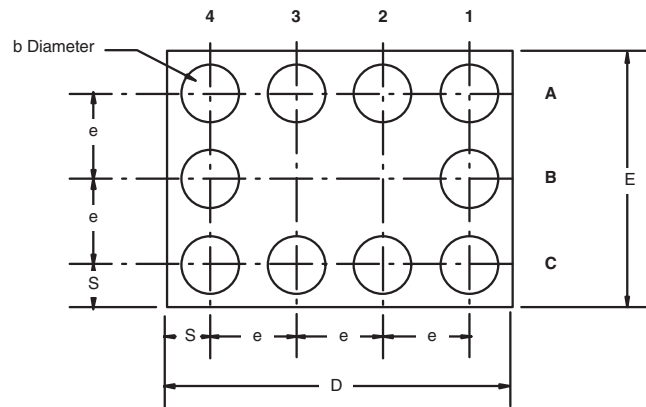
MICRO FOOT: 10-BUMP (4 mm x 3 mm, 0.5 mm PITCH, 0.238 mm BUMP HEIGHT)



Recommended Land Pattern



Top Side (Die Back)



Notes

(unless otherwise specified)

- a. Bump is lead (Pb)-free Sn/Ag/Cu.
- b. Non-solder mask defined copper landing pad.
- c. Laser mark on silicon die back; back-lapped, no coating. Shown is not actual marking; sample only.

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S	0.230	0.270	0.0091	0.0106

Note

- a. Use millimeters as the primary measurement.

ECN: S11-1065-Rev. A, 13-Jun-11
 DWG: 6001



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