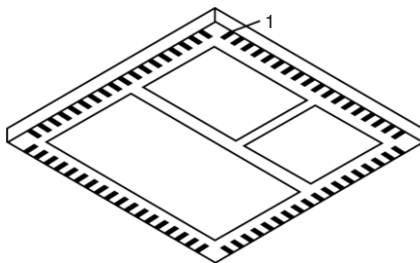


## Fast Switching MOSFETs With Integrated Driver

PRODUCT SUMMARY	
Input Voltage Range	3.3 to 16 V
Output Voltage Range	0.5 to 6 V
Operating Frequency	100 kHz to 1 MHz
Continuous Output Current	Up to 25 A
Peak Efficiency	> 96 % at 300 kHz
Optimized Duty Cycle Ratio	40 %

PowerPAK® MLF 10 x 10



Bottom View

Ordering Information: SiC711CD10-T1  
SiC711CD10-T1-E3 (Lead (Pb)-free)  
\*see page 2 for peak temperature

### FEATURES

- Low-side MOSFET control pin for pre-bias start-up
- Undervoltage Lockout for safe operation
- Internal bootstrap diode reduces component count
- Break-Before-Make operation
- Turn-on/Turn-off Capability
- Compatible with any single or multi-phase PWM controller
- Low profile, thermally enhanced PowerPAK® MLF 10 x 10 Package



Available  
**RoHS\***  
COMPLIANT

### APPLICATIONS

- DC-to-DC Point-of-Load Converters
  - 3.3 V, 5 V, or 12 V Intermediate BUS
  - Examples
    - 12 V<sub>IN</sub>/3.3 - 5 V<sub>OUT</sub>
    - 5 V<sub>IN</sub>/1.5 - 3.3 V<sub>OUT</sub>
    - 3.3 V<sub>IN</sub>/1.0 - 2.5 V<sub>OUT</sub>
- Servers and Computers
- Single and Multi-Phase Conversion

### DESCRIPTION

The SiC711CD10 is an integrated solution which contains two PWM-optimized MOSFETs (high side and low side MOSFETs) and a driver IC. Integrating the driver allows better optimization of Power MOSFETs. This minimizes the losses and provides better performance at higher frequency.

The SiC711CD10 is packed in Vishay Siliconix's high performance PowerPAK MLF 10 x 10 package. Compact co-packing of components helps to reduce stray inductance, and hence increases efficiency.

### FUNCTIONAL BLOCK DIAGRAM

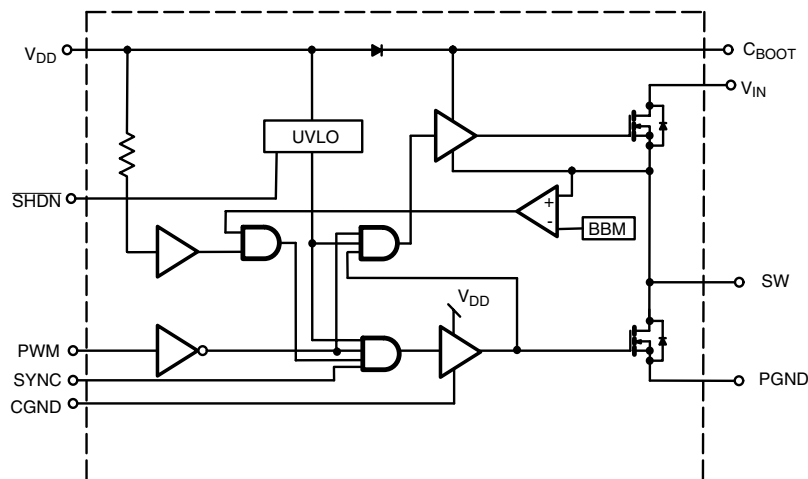


Figure 1.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted			
Parameter	Symbol	Steady State	Unit
Logic Supply	$V_{DD}$	7	V
Logic Inputs	$V_{PWM}$	7.3	
Common Switch Node	$V_{SW}$	30	
Drain Voltage	$V_{IN}$	20	
Bootstrap Voltage	$V_{BOOT}$	SW + 7	
Maximum Power Sissipation (Measured at 25 °C )	$P_D$	6	W
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	- 65 to 125	°C
Soldering Recommendations (Peak Temperature) <sup>a, b</sup>		240	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

<b>RECOMMENDED OPERATING CONDITIONS</b>			
Parameter	Symbol	Steady State	Unit
Drain Voltage	$V_{IN}$	3.0 to 16	V
Logic Supply	$V_{DD}$	4.5 to 5.5	
Input Logic PWM Voltage	$V_{PWM}$	5	
Bootstrap Capacitor	$V_{BOOT}$	100 n to 1 $\mu$	F

<b>THERMAL RESISTANCE RATINGS</b>					
Parameter <sup>c</sup>		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Case	Steady State	$R_{thJC}$	2.1	2.6	°C/W
Maximum Junction-to-Ambient (PCB = Copper 25 mm x 25 mm)		$R_{thJA}$	50	75	

## Notes:

- See Reliability Manual for profile. The PowerPAK MLF 9 x 9 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot guaranteed and is not required to ensure adequate bottom side soldering interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Junction-to-case thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ( $R_{thJA} = R_{thJC} + R_{thPCB-A}$ ). It can also be used to estimate chip temperature if power dissipation and the lead temperature of heat carrying (drain) lead is known.

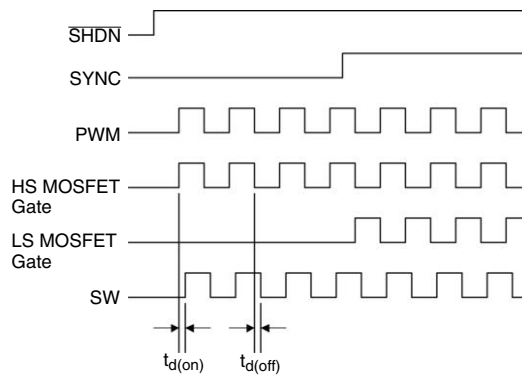


<b>SPECIFICATIONS</b>							
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25\text{ }^\circ\text{C}$ $4.5\text{ V} < V_{DD} < 5.5\text{ V}, 4.5\text{ V} < V_{D1} < 20\text{ V}$	Limits			Unit	
			Min	Typ <sup>a</sup>	Max		
<b>Controller</b>							
Logic Voltage	$V_{DD}$		4.5		5.5	V	
Logic Current (Static)	$I_{DD(EN)}$	$V_{DD} = 4.5\text{ V}, \text{SYNC} = \text{H}, \text{PWM} = \text{H}, \overline{\text{SHDN}} = \text{H}$		1072		$\mu\text{A}$	
	$I_{DD(DIS)}$	$V_{DD} = 4.5\text{ V}, \text{SYNC} = \text{H}, \text{PWM} = \text{H}, \overline{\text{SHDN}} = \text{L}$		122			
Logic Current (Dynamic)	$I_{DD1(DYN)}$	$V_{DD} = 5\text{ V}, f_{\text{clk}} = 250\text{ kHz}^c$		10		mA	
	$I_{DD2(DYN)}$	$V_{DD} = 5\text{ V}, f_{\text{clk}} = 0.7\text{ MHz}^c$		39			
<b>Logic Input</b>							
Logic Input (VPWM)	High	$V_{\text{PVMH}}$	$V_{DD} = 5\text{ V}, \text{SYNC} = \text{H}, \overline{\text{SHDN}} = \text{H}$	2.5		V	
	Low	$V_{\text{PVM L}}$			1.35		
Logic Input Voltage ( $V_{\text{SYNC}}$ )		$V_{\text{SYNC}}$	$V_{DD} = 5\text{ V}, \text{PMW} = \text{H}, \overline{\text{SHDN}} = \text{H}$		2.0		
Logic Input Voltage ( $V_{\text{SHDN}}$ )		$V_{\text{SHDN}}$	$V_{DD} = 5\text{ V}, \text{PMW} = \text{H}, \text{SYNC} = \text{H}$		2.0		
Input Voltage Hysteresis (PWM)		$V_{\text{HYS}}$			400	mV	
Logic Input Current		$I_{\text{SHDN}}$	$V_{DD} = 5.5\text{ V}, \overline{\text{SHDN}} = 0\text{ V}$		120	$\mu\text{A}$	
		$I_{\text{PWM}}$	$V_{DD} = 5.5\text{ V}, \text{PMW} = 5.5\text{ V}$		120		
<b>Protection</b>							
Break-Before-Make Reference		$V_{\text{BBM}}$	$V_{DD} = 5.5\text{ V}$		2.4	V	
Under-Voltage Lockout		$V_{\text{UVLO}}$	$V_{DD} = 5\text{ V}, \text{SYNC} = \text{H}, \overline{\text{SHDN}} = \text{H}$	3.5	4		4.25
Under-Voltage Lockout Hysteresis		$V_{\text{H}}$			0.4		
<b>MOSFETs</b>							
Drain-Source Voltage		$V_{\text{DS}}$	$I_D = 250\text{ }\mu\text{A}$	20	24	V	
Drain-Source On-State Resistance <sup>a</sup>		$r_{\text{DS(on)1}}$	$V_{DD} = 5\text{ V}, I_D = 10\text{ A}$ $T_A = 25\text{ }^\circ\text{C}$	High-Side	4	5.0	m $\Omega$
		$r_{\text{DS(on)2}}$		Low-Side	4	4.8	
Diode Forward Voltage <sup>a</sup>		$V_{\text{SD1}}$	$I_S = 2\text{ A}, V_{\text{GS}} = 0\text{ V}$	High-Side	0.7	1.1	V
		$V_{\text{SD2}}$		Low-Side	0.7	1.1	
<b>Dynamic<sup>b, c</sup></b>							
Turn On Delay Time		$t_{\text{d(on)}}$	50 % - 50 % <sup>c</sup>		60	ns	
Turn Off Delay Time		$t_{\text{d(off)}}$			57		

Notes:

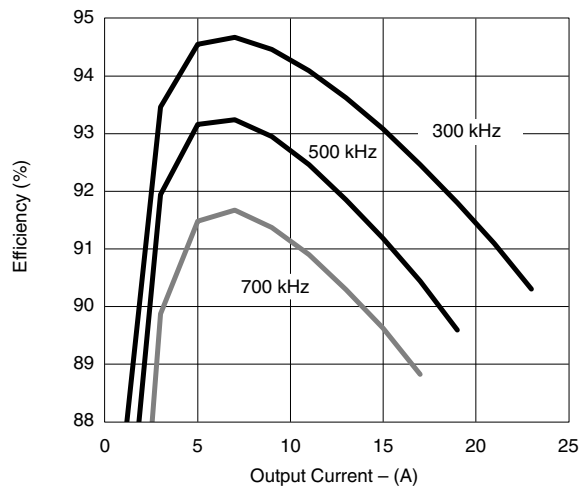
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. Using application board SiDB766707.

**TIMING DIAGRAM**

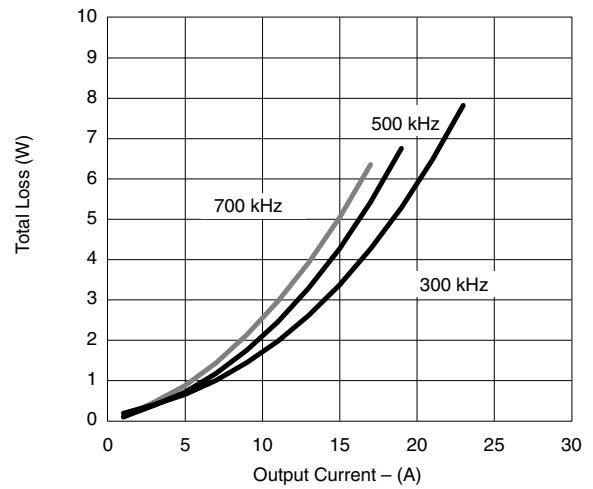


**Figure 2.**

**APPLICATION INFORMATION<sup>a</sup>** (25 °C, unless noted, LFM = 0)



**Figure 3. Total Efficiency 12 V<sub>IN</sub>/3.3 V<sub>OUT</sub>**

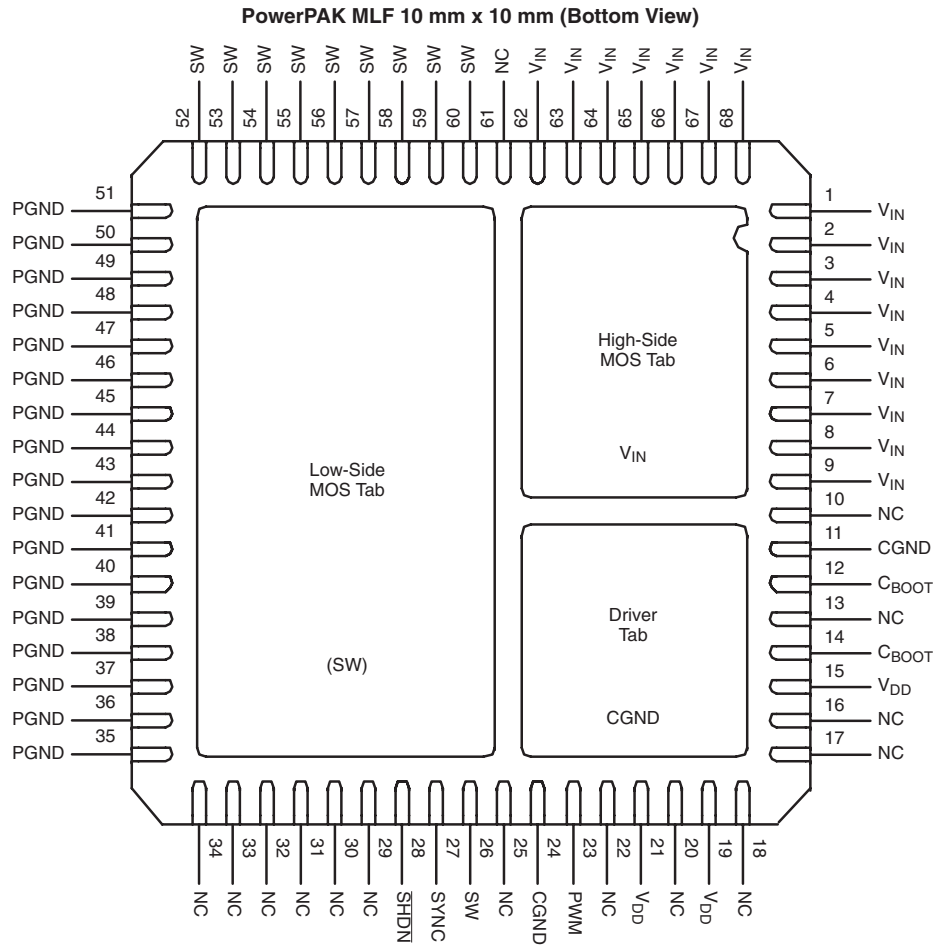


**Figure 4. Total Loss 12 V<sub>IN</sub>/3.3 V<sub>OUT</sub>**

Notes:

a. Experimental results using an evaluation board with a specific set of operating conditions.

**PIN CONFIGURATION**



<b>TRUTH TABLE</b>				
SHDN	SYNC	PWM	HS MOSFET	LS MOSFET
L	X	X	OFF	OFF
H	L	L	OFF	OFF
H	L	H	ON	OFF
H	H	L	OFF	ON
H	H	H	ON	OFF

<b>PIN DESCRIPTION</b>		
Pin Number	Symbol	Description
1 - 9, 62 - 68	$V_{IN}$	Input-Voltage (High-Side MOSFET Drain)
10, 13, 16 - 18, 20, 22, 25, 29 - 34, 61	NC	No Connect
11, 24	CGND	Control Ground. Should be connected to PGND externally
12, 14	$C_{BOOT}$	Connection Pin for Bootstrap Capacitor for Upper MOSFET
15, 19, 21	$V_{DD}$	Logic Supply Voltage - decoupling to GND with a CAP is strongly recommended
23	PWM	Pulse Width Modulation (PWM) signal Input
27	SYNC	Disable Low-Side MOSFET Drive
28	SHDN	Disable All Functions (Active low)
35 - 51	PGND	Power Ground (Low-Side MOSFET Source)
26, 52 - 60	SW	Connection Pin for Output Inductor (High-Side MOSFET Source/Low-Side MOSFET Drain)

## DEVICE OPERATION

### Pulse Width Modulator (PWM)

This is a CMOS compatible logic input that receives the drive signals from the controller circuit. The PWM signal drives the buck switch.

### Break-Before-Make (BBM)

The SiC714CD10 has an internal break-before-make function to ensure that both high-side and low-side MOSFETs are not turned on the same time. The low-side MOSFET will not turn on until the high-side gate drive voltage is less than  $V_{BBM}$ , thus ensuring that the high-side MOSFET is turned off. This parameter is not user adjustable.

### $\overline{\text{SHDN}}$

CMOS logic signal. In the low state, the  $\overline{\text{SHDN}}$  disables both high-side and low-side MOSFET's.

### Capacitor to Boot Input ( $C_{BOOT}$ )

Connected to  $V_{DD}$  by an internal diode via the  $C_{BOOT}$  pin, the boot capacitor is used to sustain rail for the high-side MOSFET gate drive circuit.

### Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET's low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The UVLO is not user adjustable.

## APPLICATION CIRCUIT

**Power Up Sequence:** The presence of  $V_{DD}$  prior to applying the  $V_{IN}$  and PWM is recommended to ensure a safe turn on

**Power Down Sequence:** The sequence should be reverse of the on sequence, turn off the  $V_{IN}$  before turning off the  $V_{DD}$ .

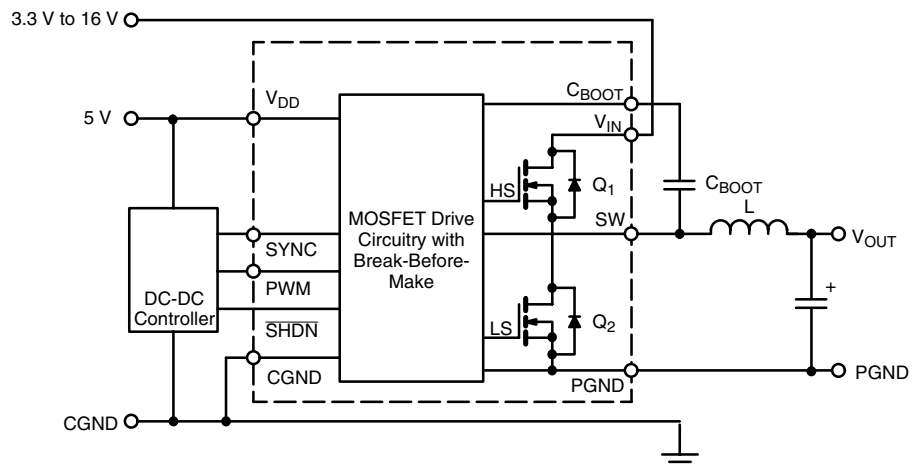


Figure 5.

The SiC711CD10 has a built-in delay time that is optimized for the MOSFET pair. When the PWM signal goes low, the high-side driver will turn off, after circuit delay ( $t_{doff}$ ), and the output will start to ramp down, ( $t_f$ ). After a further delay, the low-side driver turns on.

### SYNC Pin for Pre-Bias Start-Up

The low side MOSFET can be individually enable or disabled by using the SYNC pin. In the low state (SYNC = low), the low-side MOSFET is turned off. In the high state, the low-side MOSFET is enabled and follows the PWM input signal (see timing diagram, Figure 2). SYNC is a CMOS compatible logic input and is used for a pre-biased output voltage.

### Voltage Input ( $V_{IN}$ )

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

### Switch Node (SW)

The Switch node is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter.

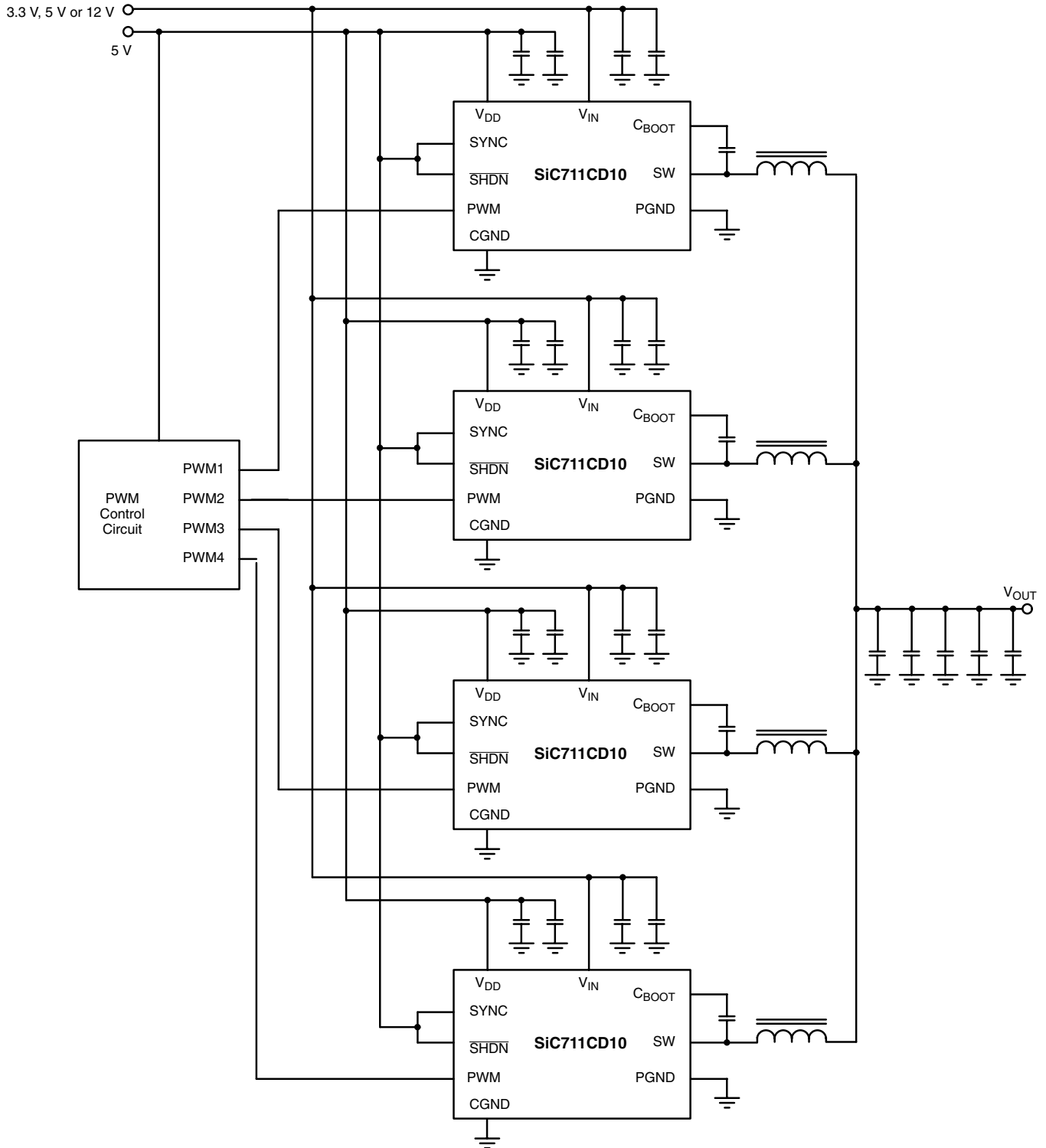
### Power Ground (PGND)

This is the output connection from the source of the low-side MOSFET. This output is the ground return loop for the power rail. It should be externally connected to CGND.

### Control Ground (CGND)

This is the control voltage return path for the driver and logic input circuitry to the SiC711CD10. This should externally connected to PGND.

**TYPICAL APPLICATION**



**Figure 6.**

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