Development of a Lead (Pb)-Free Soldering Process for PolarPAK

By Kandarp Pandya

ABSTRACT

PolarPAK is one of the latest Vishay Siliconix SMD packages with enhanced thermal efficiency. Heat from the semiconductor MOSFET chip is removed from both the top and bottom surfaces. This article describes the development of a lead-free and tin-lead (Sn-Pb) soldering process.

The design of experiment (DOE) is actually the first phase of a solder joint reliability evaluation that studies thermal fatigue [1]. However, the purpose of this exercise is to develop an assembly process while trying to understand the impact of two process parameters - stencil design and reflow profile - on solder release and voids in a solder joint for leadless components using lead-free solder. The target area percentage of voids is less than 25%. The PC board under test is designed with IPC-9701 [2], the guidelines for SMD solder joint reliability. The intent is to develop recommended assembly processes for both lead-free and tin-lead solder pastes.

The experiments were done at a third-party, contract-manufacturing facility. Current industry-standard assembly practices and equipment setups were used to insure a smooth implementation of results in manufacturing practices. The best recommended lead-free and Sn-Pb solder pastes were selected. Varieties of reflow profiles used are ramp-to-spike (RTS), ramp-soak-spike (RSS), and ramp-long-soak-spike (LRSS). Other process variables are stencil designs, solder paste applicator machine parameters, and those for part pick-and-place machine. Both 5DX laminography X-ray and 2DX transmission X-ray equipment were used for data collection and analysis.

This DOE comprises a minimal but adequate component sample size that would enable the researchers to arrive at a reasonable conclusion. The measuring bar is the minimum void area percentage of a solder joint estimated from X-ray data. Based on the latter, the conclusions and recommendations define guidelines for the selection of process parameters such as stencil aspect ratio, aperture opening, machine operating parameters, and reflow profile.

PROCESS DEVELOPMENT PHASE OVERVIEW:

(a) The main objective is to develop a recommended reflow process that can assemble a new generation of PolarPAK: Vishay leadless packages on a 3.175-mm [0.125-in.] thick, 16-layer PCB with voids level less than 25%
(b) Use two process parameters: reflow profile and stencil aperture
(c) Experiment with three different reflow profiles and four stencil apertures
(d) Use 20 PCBs
(e) Examine and evaluate X-rays, adjust parameters, and repeat the assembly to obtain the best possible results that will enable recommendations

EQUIPMENT AND MATERIAL:

1) EKRA E5 solder paste printer
2) Juki E2060 pick and place machine
3) BTU Pyramax 98 reflow oven
4) Agilent 5DX Series 5300 laminography X-ray
5) Nicolet NXR-1400 transmission X-ray
6) 30x microscope
7) Lead (Pb)-free solder paste SAC-387 (Tamura TLF-206-93G)
8) Tin-lead (Sn-Pb) no-clean solder paste Sn63-Pb37 (Alpha Metal UP78)
9) 4-mil and 5-mil stencils with a variety of aperture and aspect ratios
10) Vishay PolarPAK components
11) Vishay Siliconix PCB version SMD125T16L_Ver C Side A (see Appendix D for board layout details and Appendix E for PCB fabrication details)

EXPERIMENTS:

With a primary focus on a process development for a reflow profile using lead (Pb)-free solder, 18 runs were designed using 14 boards. The intent was to gather adequate data to be able to draw a reliable conclusion. This was imperative due to many unknown variables such as the new-generation package, almost worst-case PCB design comprising 3.175-mm [0.125-in.] thick, 16-layer board with 70% to 100% copper on internal layers, and lead (Pb)-free solder paste. Reusing the PCB during repeat reflow after parameter adjustments optimized its utilization.

To clarify the nomenclature definition for PCB sides, consider an example name of Side CA. The letter "C" identifies version C of PCB version A, B or C, while the letter "A" identifies side A between two sides, A and B, of a PCB.

Reflow profile definitions:

Ramp-to-spike	RTS
Ramp-soak-spike	Reg RSS
Ramp-long-soak-spike	Long RSS

Table 1

Board #	Side	Comp Type	Profile	Build Sequence	Stencils
1	CA	PolarPAK	RTS	First	5 mils
2	CA	PolarPAK	Reg RSS	First	5 mils
12	CA	PolarPAK	Long RSS	Single	5 mils

To establish a baseline with tin-lead (Sn-Pb) solder paste, two PCBs were assembled using a pre-established reflow profile using a 5-mil stencil.

PROCESS PARAMETERS:

a. Reflow profiles:
Selection criteria:

1. RTS (ramp-to-spike): This is a straight ramp profile, mostly used for small boards with equal mass distribution.
2. Reg RSS (regular ramp-soak-spike): This is a soak profile mostly used for boards with different component mass.
3. Long RSS (ramp-long-soak-spike): This is a soak profile with extended soak time.

Details of different profiles used in this experiment are shown in figures 1 through 3 for lead (Pb)-free solder paste and Figure 4 for tin-lead solder paste.

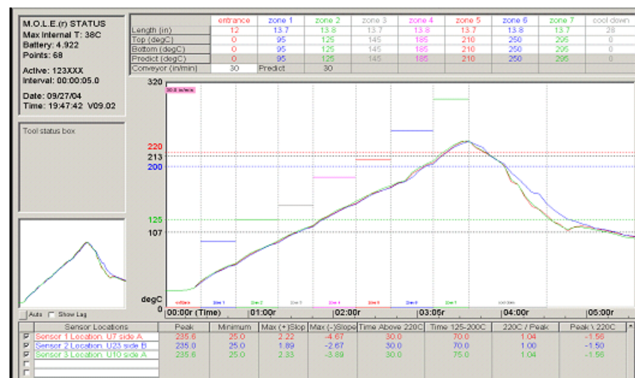


Figure 1: RTS Profile for lead (Pb)-free solder paste
Peak temperature: 235 °C
Time above 220 °C: 30 seconds
Soak time (120-200 °C): 70 seconds

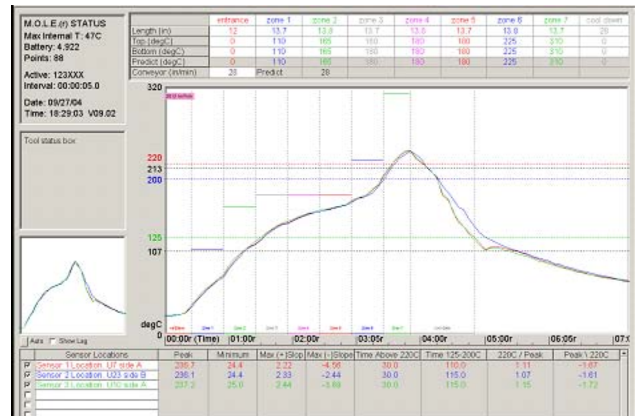


Figure 2: RSS profile for lead (Pb)-free solder paste
Peak temperature: 237 °C
Time above 220 °C: 30 seconds
Soak time (120-200 °C): 115 seconds

Figure 3: LRSS profile for lead (Pb)-free solder paste
Peak temperature: 235 °C
Time above 220 °C: 32 seconds
Soak time (120-200 °C): 159 seconds

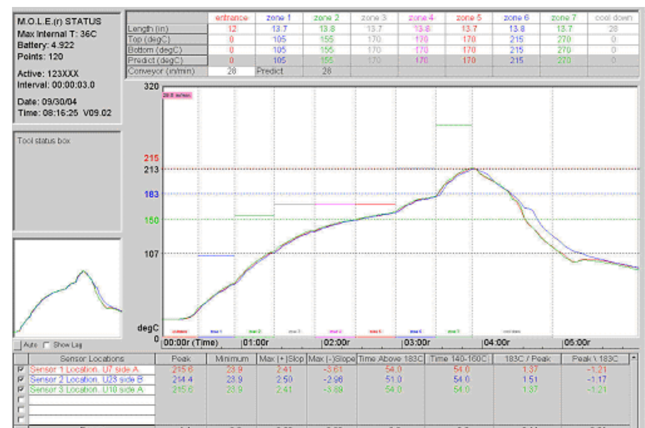


Figure 4: RSS profile for tin-lead (Sn63/Pb37) solder paste
Peak temperature: 215 °C
Time above 183 °C: 54 seconds
Soak time (140-160 °C): 54 seconds

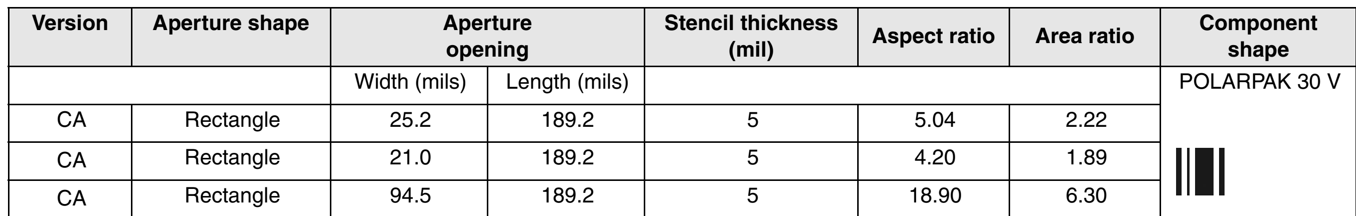
b. Stencil aperture opening:

Four different apertures for signal pins were studied:

1) 1:1 - same as the size of the pad
2) Component - same as the size of the component termination
3) Reduce 10% - aperture reduction from the pad size
4) Increase 10% - aperture increase from the pad size

c. Aperture shape and size, stencil thickness, and aspect ratio are described in the following table:

Table 2



Version	Aperture shape	Aperture opening		Stencil thickness (mil)	Aspect ratio	Area ratio	Component shape
		Width (mils)	Length (mils)				POLARPAK 30 V
CA	Rectangle	25.2	189.2	5	5.04	2.22	
CA	Rectangle	21.0	189.2	5	4.20	1.89	
CA	Rectangle	94.5	189.2	5	18.90	6.30	

METHODOLOGY:

Two methods were employed to determine the best process parameters:

1. 2DX image review, in which all image void levels were compared and ranked. Signal pads and ground pads were compared independently. The focus was on the number and size of voids.
   a. Profile selection - each reference designator from two or more boards was compared and ranked. The best image has the lowest rank.
   b. Stencil aperture selection - all reference designators per component type per board were compared and ranked from 1 to 8. The best image has the lowest score.
2. 5DX void measurement, in which all voids measurements obtained from the 5DX were sorted and selected based on the percentage of the void area. Signal pads and ground pads are compared independently.

The first method, 2DX image review, was a qualitative comparison. The second method, 5DX parametric data, was a quantitative analysis. Both methods have their own pros and cons. 2DX image comparisons are subjective, whereas the 5DX parametric database may have some false calls due to the noise level, especially from the pins with smaller aperture openings. Any insufficient solder or a reduction in solder coverage will be reflected as a large void; however, conclusions from the 2DX can be easily substantiated by the data from the 5DX. However, the 5DX data has added value in detailed solder joint analysis after temperature cycling. Cross-sectional and volumetric information from the 5DX database are very valuable.

RESULTS:

Table 3 below summarizes the recommendable process parameters for assembly of the PolarPAK package. The selection is based on a comparison of the 2DX images and 5DX parametric database. Using these combinations, good solder release was achieved with a void level less than 25%.

Table 3

Design	Comp Type	Profile	Stencil Thickness	Aperture Design
				Signal
				Best
CA	POLARPAK	RSS	5 mils	Component

Appendix A contains the X-ray images for the best-case and the worst-case void levels for the PolarPAK package. For convenience, profile and aperture information is also noted therein.

CONCLUSIONS AND RECOMMENDATIONS:

- The minimum acceptable aspect ratio (smallest aperture opening / stencil thickness) is 2.5
- The minimum acceptable area ratio (LxW / 2(L+W)T) is 0.8
- The RSS profile shown in Figure 2 is recommended for lead-free solder paste
- The RSS profile shown in Figure 4 is recommended for tin-lead solder paste

ACKNOWLEDGMENT:

The author wishes to acknowledge the engineering contributions by NBS Design, Inc. of Santa Clara, California by way of their role as third-party vendor and contract manufacturers. Individual contributors are Jacob Djaja, Peter Chipman, Hoang Phan, and Son Ngo.

VISHAY®

REFERENCE:

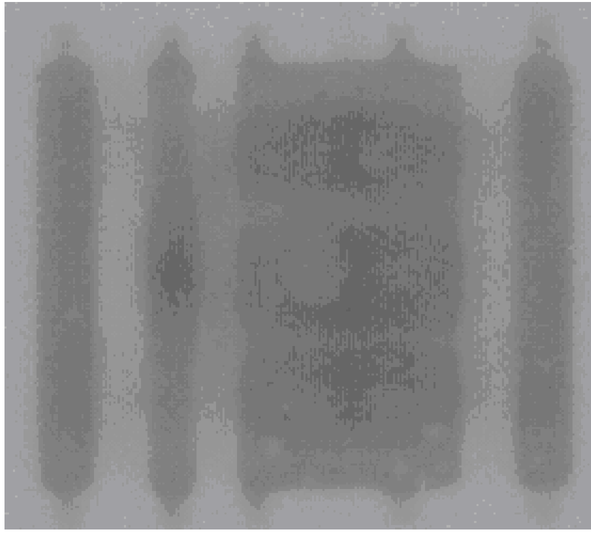
[1] "Thermal fatigue analysis to study solder joint reliability for new-generation SMD parts introduced by Vishay Siliconix," by Serge Jaunay and Kandarp Pandya.

[2] IPC-9701 Standard for Solder Joint Reliability, an IPC publication.

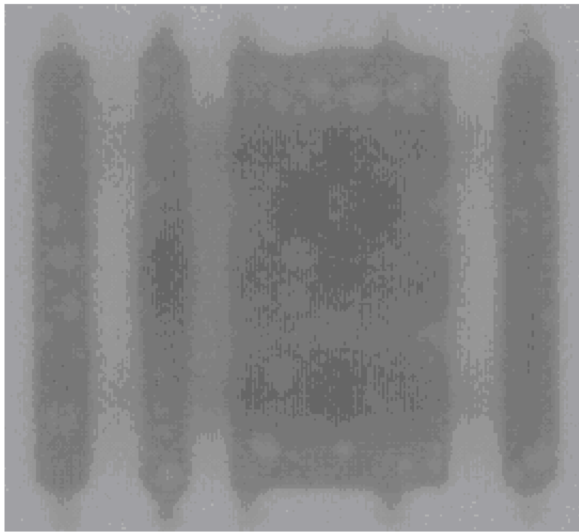
[3] "Voiding: Occurrence and reliability issues with lead-free," by Martin Wickham, NPL.

Appendix A

PolarPAK X-Ray Images



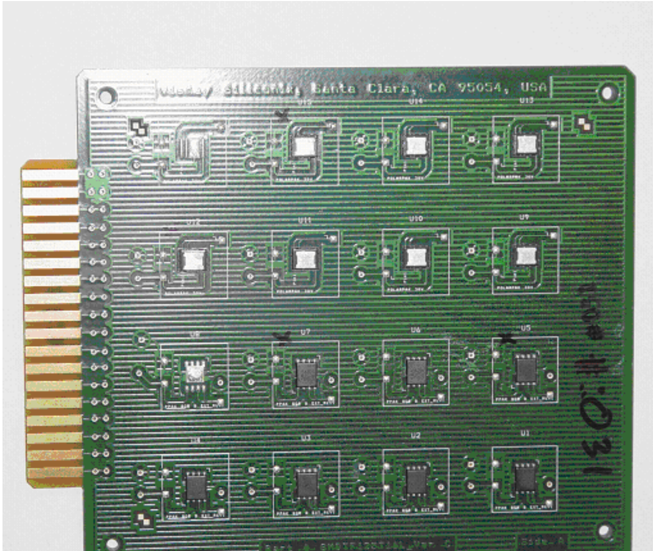
Smallest void on signal/ground pads, U15-1Profile: RTS
Aperture: Component

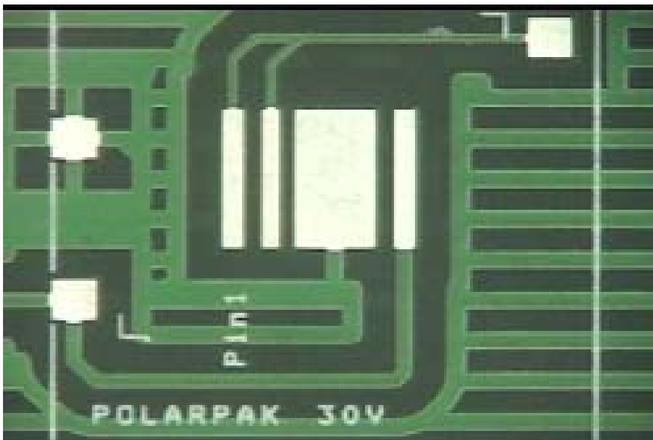


Largest void on signal/ground pads, U9-2 Profile: RSS
Aperture: Increase 10%

Appendix B

PCB Layout
SMD125T16L_Ver C_Side A





Appendix C

PCB Fabrication

Material:	FR-4
Thickness:	3.175 mm [0.125 in.]
Number of copper (Cu) layers:	16
Nominal outer layer (top/bottom) Cu thickness:	35 μm [1378 μin.] ½ oz.
Nominal inner layer Cu thickness:	12 μm [472 μin.] ½ oz.
Nominal FR4 insulation layer thickness:	231.8 μm [7709 μin.]
Even internal layers 2, 4, 5, 7 from each side:	Power and ground
Cu coverage on power/ground layers:	70%
Cu coverage on signal trace:	40%
Minimum outer layer trace width:	150 μm [5906 μin.]

Test pads for each daisy chain to be provided

Minimum 15-mm [0.6-in.] clearance around each part for rework and if necessary removal of a failed part without damage to the adjacent part/trace

Minimum via for large (drain) land pad:	50%
Via size: Pitch:	1.0 mm [0.040 in.]
Diameter:	0.3 mm [0.012 in.]

Solder mask encroach on via pad for these via on the bottom side. This will prevent the solder from spreading on the bottom side.

Square test pad size:	1.5 mm [0.060 in.]
PTH Drill:	1.0 mm [0.040 in.]
Surface finish: (preferred)	OSP (Organic Solderability Preservative)

Silkscreen or Cu etch to label all components, all test points, and location of pin is mandated.