

Evaluation Board for the Vishay Siliconix Si9122 Half-Bridge DC-DC Controller IC with Primary-Side Synchronous Rectifier Control

INTRODUCTION

The Si9122 Evaluation Board ("Eval Board") demonstrates the Vishay Siliconix Si9122 controller in a typical DC-to-DC converter application. The module is shipped from the factory configured for an output of 2.5 V at 40 A, but can readily provide other output voltages and currents with only a few component changes:

- 3.3 V at 30 A
- 1.8 V at 50 A
- 1.5 V at 50 A
- 1.225 V at 50 A

The Eval Board's input voltage spans the normal telecommunications voltage range of 36 V to 72 V.

The Eval Board is implemented using planar magnetics on a 10-layer board, in a form factor similar to standard "brick" type converters. A somewhat larger footprint was chosen to allow for user access to component terminals, and for provision of test points and some optional device positions. The end user can therefore design a smaller form factor converter with the Si9122 controller, having a reduced component count, to meet specific market requirements.

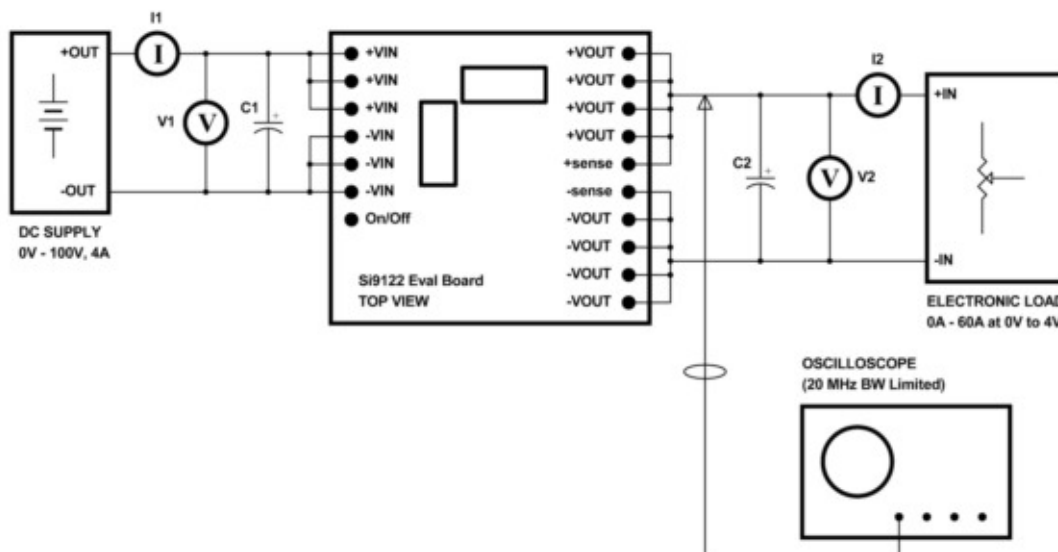
This Evaluation Board is intended to provide a functional application circuit for use by persons experienced in the design and testing of power converters. As a necessary result of this, voltages in excess of "Safety Extra Low Voltage" (SELV) levels may be present on the Eval Board, and high

operating temperatures may also be experienced. This Eval Board is further specifically designed to allow modification by such users, which may lead to operating conditions not in accordance with initial design parameters.

Performance measurements will normally be undertaken with a bench power supply connected to the +V_{IN} and -V_{IN} terminals, and a load connected to the +V_{OUT} and -V_{OUT} terminals. The +Sense and -Sense terminals will normally be connected to the corresponding output terminals (+V_{OUT} and -V_{OUT} respectively). Operation with remote sensing of the output voltage is treated later in the "circuit description" section. An ON/OFF pin is provided if operation with an external signal control is required.

Ripple and noise measurements are ordinarily performed across the output with a 10 μF capacitor connected across the oscilloscope probe and ground, and with use of short ground lead on the oscilloscope. Use of a common-mode filter choke on the oscilloscope leads (typically implemented by winding the oscilloscope probe lead for 3 turns through a high-permeability ferrite toroid) will make possible more meaningful measurements of low level signals such as ripple, noise and transient response.

The typical evaluation setup is as shown.



Equipment List:

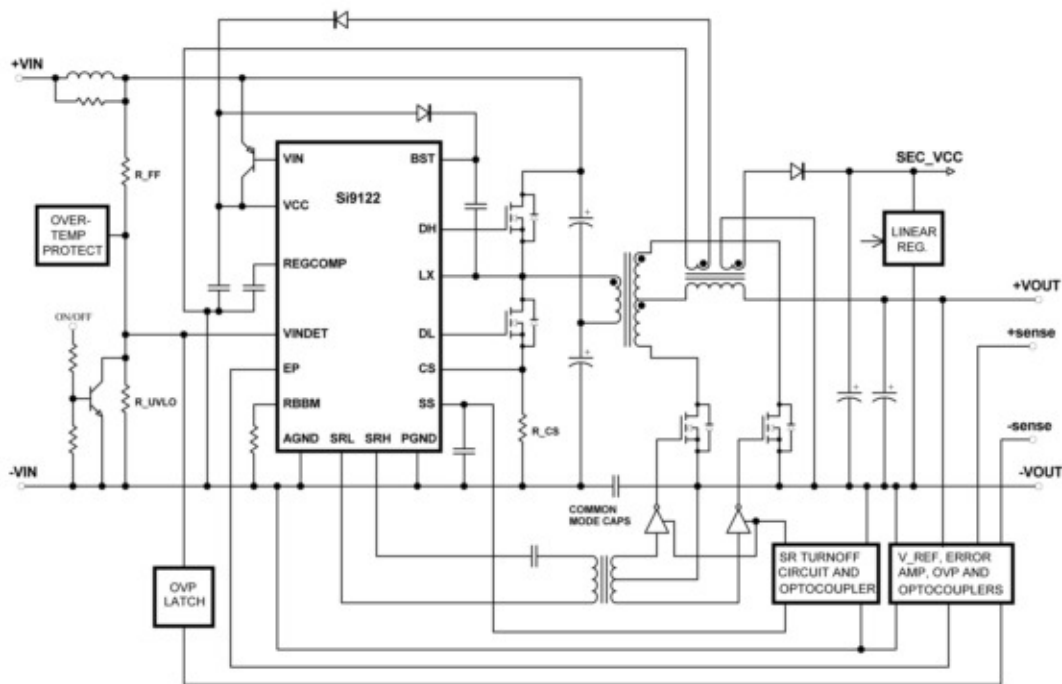
- V1 is a voltmeter with a 0 V - 100 V range
- V2 is a voltmeter with a 0 V - 5 V range (in practice, 0 V - 20 V is more common)
- I1 is an ammeter with a 0 A - 4 A range (or a 5 A current shunt and a voltmeter)
- I2 is a 60 A current shunt and voltmeter combination (50 A is acceptable if the Eval Board will only be used in its 2.5 V and/or 3.3 V output configurations)
- C1 is a 100 μ F, 160 V electrolytic capacitor (for use with long power supply leads)
- C2 is a 10 μ F, 6.3 V ceramic capacitor. Connected C2 from +V_{OUT} to -V_{OUT} when performing ripple and noise measurements.

The converter pins use industry-standard headers, which will mate with standard 5.08 mm (0.200") pitch sockets. If sockets are used, connections should be minimized by using all four output pins for each of +V_{OUT} and -V_{OUT}. Attention should also be given to socket heating effects, which may affect the thermal performance of the module. When full rated output currents are being drawn from the converter, it is recommended that soldered connections be made to the output pins.

Users wishing to modify the Eval Board beyond the programming and configurability described herein can use up to 4 input-stage MOSFETs and 6 synchronous rectifier MOSFETs. The performance of Si9122-driven controllers operating over a wide range of conditions may thereby be investigated using this Eval Board.

BLOCK DIAGRAM

A block diagram for the controller is given below.



Si9122 Eval Board Block Diagram

CIRCUIT DESCRIPTION**Input Filter Elements**

Input current, at any voltage between 36 V and 72 V, enters via the input pins. From the input pins, this current first passes through a fuse. The fuse is a 5 A, 125 V rated type in a surface-mount fuse holder. In most commercially manufactured converters such a fuse would be provided externally.

The input voltage is then fed through an input filter inductor L2 (1.5 μ H), which is damped by resistor R14 (4.7 Ω). This damping resistor serves to prevent ringing, which could otherwise occur between the input inductor and the input capacitors.

The evaluation board will normally be operated from a low-impedance source. To guarantee low impedance at the relevant frequencies, connecting a 100 μ F electro-

lytic capacitor with a low ESR across to the input terminals is recommended there is a long lead run to the input power supply.

The input capacitors are configured as the series connection of two groups of parallel capacitors, as is appropriate for the half-bridge topology employed. The upper capacitor bank comprises C15, C16, C45 and C46 and the lower bank comprises C17, C18, C19 and C20. Each of these capacitors is nominally 1.5 μF at 50 V. Resistors R19 and R20 (each 100 k) are provided to ensure voltage balance across each capacitor group on startup and during shutdown.

Switching Power Train Components

The converter uses Q3A and Q3B as the upper (high-side) switching elements in the half-bridge circuit, and Q4A and Q4B as the low-side devices. At power levels up to 100 W, it will ordinarily be sufficient to use a single device such as the Si7456DP in each position. These devices have a maximum on-state resistance ($R_{\text{DS(ON)}}$) of 25 milli-ohms at 25 °C with a 10 V gate drive. A somewhat higher $R_{\text{DS(ON)}}$ will apply at full operating temperature.

In the Eval Board as stuffed, R60 and R5 determine the rate of turn-on of the input stage FET devices Q3A/b and Q4A/B respectively, with diodes D2 and D12 providing the turn-on current and transistors Q15 and Q16 ensuring rapid turn-off. R60 and R5 are selected to minimize switching losses and optimize EMI performance. The input stage gate drives may be implemented optionally as direct resistor drives from the controller, by making the series combination of (R59 and R60) and that of (R4 and R5) each a small value and omitting the associated diode and transistor, or by having a PNP pull-down circuit as shown, where R4 and R59 are omitted.

The output synchronous rectifiers are implemented as parallel combinations of up to three PowerPAKs™ in two positions (Q5 A/B/C and Q6 A/B/C). The Si7880ADP is used, with an $R_{\text{DS(ON)}}$ at 25 °C of 4.0 milli-ohms at $V_{\text{GS}} = 4.5 \text{ V}$, and 3 milli-ohms at $V_{\text{GS}} = 10 \text{ V}$. At operating temperatures a somewhat higher $R_{\text{DS(ON)}}$ will be observed. As shipped, the Eval Board is populated with all three devices in each output leg. Under normal operating conditions, the devices will be driven from a gate voltage of about 6 V.

The gate drive to these output rectifier devices is provided by totem pole stages, with PNP pull-down devices (Q18/Q19) and with NPN pull-up devices (Q20/Q21). Each stage is driven by a MOSFET (implemented as a dual device Si1900DL, Q17) with resistive pull-up (R49 and R67, each 270 Ω).

The input signals to Q17 come from the gate drive transformer, implemented in planar magnetic technology. The gate drive transformer is implemented as shown on the artwork, with four layers (24 turns total across layers 2, 4, 7, and 9) assigned to the primary and four layers with 5 turns each (20 turns total across layers 3, 5, 6 and 8) assigned to the center-tapped secondary. The transformer's turns ratio is therefore 24:10:10. The nominal 10 V differential level between SRH and SRL thus creates a secondary voltage of 4.2 V. A planar transformer with E14 core set is used in this application with A_L of circa 1 μH minimum, and a cross-sectional area of 14.5 mm^2 .

The magnetizing inductance of the primary winding can be calculated as 576 μH minimum. Assuming a worst-case 95% duty cycle at 250 kHz, while operating with 13 V on the primary (which equates to 52 V- μs), this yields a peak-to-peak magnetizing current of 86mA, or 43 mA peak. This is well within the capabilities of the drivers in the Si9122 for the SRL and SRH pins.

Under these conditions the peak flux is given by $50 \text{ V}_{\text{us}} = 24 * 14.5 \text{ mm}^2 * \Delta B_{\text{PK-PK}}$, giving a peak-peak flux swing of 143 mT or 72 mT peak, which this core can readily accommodate.

The Si9122 can operate at lower frequencies under current limit conditions (the "frequency foldback" feature), but this condition implies that the duty cycle has been reduced to 12.5 %. Therefore, the above analysis reflects the worst-case condition for this converter.

Component pairs R84 (100 Ω), C57 (100 pF) and R83 (100 Ω), C56 (100 pF) serve to filter any high-frequency noise or ringing which may appear on the rectifier control signal waveform.

Snubbing and clamping of power device voltages and currents is implemented through use of series RC networks R76 (22 Ω), C6 (470 pF) and R80 (22 Ω), C52 (470 pF) on the input stage, and by series RC networks R50 (1 Ω), C4 (10 nF) and R21 (1 Ω), C5 (10 nF) on the output stage. In addition D4 and D6 (with associated current limiting resistors R57 and R78, if required) serve the function of operating as peak-detecting elements to provide local bias feed to the output stage, and also act as clamps. These devices charge up C28 and C29 (each 220 nF), with current "bleed" from these under normal operation being through R85 and R86 (each 3.3 k), augmented by current drawn off by Q89 under abnormal or fault conditions.

Power Train Magnetic Components

The main power transformer L1 is implemented as 8 primary turns in four layers and a center-tapped secondary winding. This winding is implemented as three turns for

each section. The turns are interleaved to give minimal leakage inductance between primary and secondary and between both halves of the secondary.

The core employed is a modified version of a widely available E32 core. The core is modified to have a cross-section of 50 mm², giving a suitable aspect ratio for windings with low resistive loss and with low leakage inductance.

With a 3.3 V output at 500 kHz, the peak flux is calculated as 70 mT at 250 kHz. Allowing for a slightly higher value due to output device losses and operation at a higher output voltage using the remote sense capability, the transformer is still operating well within constraints imposed by core loss or by core saturation. The input voltage feedforward capability of the controller with corresponding duty cycle limitation also protects against any saturation risk.

The transformer is implemented using planar magnetics technology with the windings formed in the printed circuit board. The printed circuit board is implemented as ten layers of 70-micron (2 ounce) copper in an overall thickness of 2 mm. The outer layers are initially 35-micron (1 ounce), plated up to give the required 70-micron thickness. The assignment of layers is as follows:

Layer	Assignment
1 (Top)	Secondary #1
2	Primary
3	Secondary #2
4	Primary
5	Secondary #1
6	Secondary #2
7	Primary
8	Secondary #1
9	Primary
10 (Bottom)	Secondary #2

The interleaving shown above assists in getting very low values of leakage inductance between the primary and each secondary and between each of the secondary "windings". This minimizes the requirement for snubbing of spikes resulting from leakage inductance effects during switching.

The average length per turn for the primary is approximately 55mm and effective width approximates 2.5 mm, thus implying an aspect ratio of 22. With the use of 70-micron copper (0.24 milli-ohms/square), this implies a resistance per turn of 5.28 milli-ohms at 25 °C, or approximately 7 milli-ohms at operating temperature. For the secondary the average length is again 55mm

(allowing for some element of interconnect) with an effective width of approximately 6mm, giving an aspect ratio of approximately 9, for a resistance per turn at 25 °C of approximately 2.25 milli-ohms. With three layers this yields 0.75 milli-ohms per section, or approximately 1 milli-ohm at operating temperature.

In the half-bridge configuration employed, the transformer secondary conducts (on alternate windings in each half-cycle) for the full cycle, thus implying loss in the secondary windings of about 3 W with 50 A loading and just over 1 W with 30 A loading.

The transformer can be programmed so that the input winding has effectively 4, 6 or 8 turns, depending upon the desired output voltage. Size 1206 zero-ohm jumper resistors should be installed or omitted as follows:

Output Voltage	Install	Ommit	Effective DC R at operating temp (in-milli-ohms)
3.3 V (4 turns, two parallel windings)	R13, R15	R17, R18	14
2.5 V (4 turns, parallel windings)	R13, R15	R17, R18	14
1.8 V (6 turns)	R18	R13, R15, R17	42
1.5 V (8turns)	R17	R13, R15, R18	56
1.225 V (8 turns)	R17	R13, R15, R18	56

The primary loss at 3.3 V V_{OUT}, 48 V V_{IN} with a full 30 A load is calculated by estimating the RMS current during the on-time as 8.2 A, or a squared value of 67A², giving a loss of I²*R_{WINDING}*duty of 67*0.014*0.55, or 500 mW. Similar calculations can be undertaken for the other voltage configurations.

The output inductor L3 is likewise fashioned from a modified E32 core, with a 230-micron gap in the center leg. This core is somewhat larger than would be required in a typical single-output application. This reflects the range of current and voltage requirements for which this Eval Board can be configured.

7 turns are used to carry the output current, as seen from the artwork. With an average track length through the inductor of approximately 30 mm, and an effective width of 5 mm, the aspect ratio is approximately 6:1. As the resistance per square of 70-micron copper is approximately 240 micro-ohms at 25 °C, the resistance per layer is 1.5 milli-ohms. With 7 layers, the resistance is now 0.21 milli-ohms, or more realistically 0.28 milli-ohms at operating temperatures. An RMS current of 55 A (50 A DC plus a ripple component) will thus exhibit resistive

losses of 0.9 W. Locating the inductor's air gap above the board helps minimize AC fringe-flux effects, but some additional loss due to fringe and proximity effects can be expected.

Common-mode noise between input and output will be induced as a result of capacitances between input and output windings and imbalance with respect to grounds. The simplest approach in this type of converter is to connect a capacitor for common-mode noise reduction between input and output grounds, which is here implemented as the series combination of C35 and C36 (each 10 nF, with a 1.5 kV rating).

Output Capacitors

The output capacitor group comprises a number of 10 μ F, 6.3 V ceramic capacitors (C50, C53, C54, C24, C25, C26, C27), which are located close to the output of the inductor, which are augmented by 3 150 μ F, 6.3 V polymer electrolytic types (C21, C22 and C23, each). The polymer capacitors are located further from the inductor's output and thus carry significantly less ripple current.

Main Controller

The Vishay Siliconix Si9122 device performs the main controller function. The TSSOP package option is used on this Eval Board. The Si9122 supports the half-bridge topology and has numerous features suited to implementation of high-performance DC-DC converters. The drivers (including the integrated high-side driver) have 1 A drive capability, sufficient to turn off MOSFETs directly in medium power converters.

Other relevant features of the controller include -

- Current limit with frequency foldback
- Voltage feedforward
- Programmable "Break-before-make" function for setting the margins between switching of primary side devices and synchronous rectifiers
- Input amplifier configured for convenient duty cycle control
- Preregulator for Start-Up
- Internal over-temperature protection

Operating parameters of the controller are set as follows:

- **Current Limit:**
The internal current limit of the controller is set at a nominal 100 mV. Ordinarily the current waveform will exhibit a ramp about a fixed level, with the peak amplitude being dependent on the input voltage level

and the output voltage. For a set value of output voltage, some measure of compensation of the current limit point is thus desirable. Taking the case of 3.3V output, duty cycles with various values of input voltage (neglecting circuit losses) will be:

Input Voltage	36	48	75
Duty Cycle	73 %	55 %	35 %
Input voltage as transformed	4.5	6.0	9.4
V- μ s across inductor	1.75	2.97	4.25
Peak-Peak current swing across 300 nH inductor	5.8	9.9	14.2
Peak current swing in output inductor	2.9	5.0	7.1
Peak current swing in primary current sense	0.75	1.25	1.75

The final component of the current as sensed by the resistor is the magnetizing current of the transformer. This is essentially invariant with input voltage for a fixed output voltage. With the 3.3 V example again, we have four turns on the input, with an inductor having an A_L of about 1.5 μ H. The inductance is thus 24 μ H, and at 36 V in, 18 V is applied across this for 1.46 μ s. This gives a value of 1 A peak-to-peak or 500 mA peak.

The peak current in the current sense resistor for 30 A load current, to a first approximation, is thus given by:

Input Voltage	36	48	75
Load current component	7.5	7.5	7.5
Inductor peak component	0.75	1.25	1.75
Magnetizing current component	0.5	0.5	0.5
Total	8.75	9.25	9.75

An approximate compensation for this effect can be provided by biasing the CS1 input pin of the Si9122 (the differential current sense amplifier's inverting input) to approximately 10 mV at $V_{IN} = 36$ V and 20 mV at $V_{IN} = 75$ V. With the Si9122's current sense inputs fed via resistors R10 and R11 (each 330 Ω), a 10 mV offset is provided by resistor R22 (1 M for 3.3 V output) connected to the junction of CS1 and resistor R11.

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Allowing for a 90 mV minimum current limit threshold of the Si9122, the 10mV of pre-bias on the CS1 pin of 10 mV at $V_{IN} = 36$ V requires the voltage produced across the current sense resistor to be $(90 \text{ mV} + 10 \text{ mV}) = 100$ mV at 36 V, increasing to 110 mV at 75 V in. For 100 mV with 8.75 A the required current sense resistor value is 11.4 milli-ohms.

A similar analysis can be undertaken for other values of output voltage, yielding a programming table as follows:

Output Voltage	3.3	2.5	1.8	1.5	1.225
Frequency (kHz)	500	500	400	300	300
Rated Current (A)	30	40	50	50	50
R22	1 M	1.5 M	0.68 M	1.5 M	1.5 M
Total current sense resistance (milli-ohms)	11.4	8	11.4	15	15
R12 (milli-ohms)	15	15	15	15	15
R87 (milli-ohms)	33	15	47	100	33
R88 (milli-ohms)	-	-	-	-	33

C12 (100 pF) augments the on-chip leading-edge blanking in allowing for initial transient switching currents due to discharge of capacitances, reverse recovery effects, and the like.

- **Oscillator Frequency:**
Resistor R6 sets the oscillator frequency, with C30 (220 pF) providing some AC decoupling to this pin of the Si9122. The chart given in the Si9122 data sheet is used to determine R6 as follows:

Output Voltage	3.3	2.5	1.8	1.5	1.225
Nominal Frequency (kHz)	500	400	300	300	300
R6 Value (k Ω)	30	39	56	56	56

The frequencies shown are approximately optimal for each output voltage setting. Operation at lower output voltages means fewer volt-seconds are applied to the windings, giving the opportunity to increase the period (reduce the frequency), yielding a reduction in overall switching losses.

- **Break-Before-Make Programming:**
From the device datasheet and from consideration of circuit delays in driving the MOSFETs, a suitable value for R9 on this Eval Board is 27 k.

- **UVLO Implementation:**
The undervoltage lockout arrangement is necessary in order to avoid drawing excessive current and operating outside the intended control range at lower input voltages. The V_{INDET} signal is compared with the Si9122's 3.3 V reference voltage inside the IC, to provide a converter-level undervoltage lockout. The comparator inside the Si9122 has about 0.3 V of hysteresis, to avoid any system oscillations. R1 (90.9 k) and R66 (10 k) function as a voltage divider such that approximately one tenth of the input voltage appears at the V_{INDET} pin. A low-leakage Zener diode (ZD3) limits the voltage appearing on the V_{INDET} pin, for protection against high input voltage transients. C49 and C3 provide local decoupling.

A number of auxiliary protection functions function by pulling down the V_{INDET} pin. These functions are described in more detail subsequently.

- **Soft-Start:**
At converter turn-on, the Si9122's SS pin is used in conventional fashion to gradually bring up the duty cycle of the converter to its final operating level. During this period, a current of 20 μ A charges capacitor C14 to a final voltage of about 8 V.

If the Si9122 is shut down due to a fault or to loss of input voltage, the SS pin is pulled low by a MOSFET internal to the Si9122. This provides a useful flag for an unrelated but useful function: at turn-off, it is desirable to put the converter's synchronous rectifiers into diode mode very rapidly to prevent the output ringing and undershoot which can otherwise occur, especially at light load.

When the Si9122 pulls its SS pin low, R81 allows the pin to go low without the delay otherwise incurred by discharging C14. This low-going edge is coupled through C59 (470 pF) to turn on Q13, which in turn drives the phototransistor of optocoupler U6 (U6B). R82 provides a DC return path across the gate and source of Q13. R91 (3.3 k) and ZD5 (6.8 V) assist in giving stable operating conditions for the drive to U6B. This causes a current to flow in the phototransistor of the optocoupler (U6A), to develop a voltage across R55 (4.7 k). This voltage turns on MOSFET Q23, which pulls down the bases of the totem-pole drivers to the synchronous rectifier FETs via a dual PNP transistor (Q22). By this method, the SS pin forces the synchronous rectifiers into diode mode at turn-off.

- **Preregulator:**
The preregulator is implemented as shown in the Si9122 datasheet, with Q2 providing the bulk of the

required start-up current. This ensures a fast charge-up of the 50 μF of capacitance connected to the Si9122's V_{CC} pin to the part's 8.8 V (nominal) operating V_{CC} level. Once the converter starts operating, power fed back from a winding on the output inductor to the primary will cause V_{CC} to exceed the 9.1 V (nominal) preregulator turn-off voltage, and both the on-chip preregulator and Q2 will be turned off to minimize circuit dissipation. When this happens, R27 (1 M) prevents an open-base condition. R2 (0 Ω) may be fitted with a non-zero value to reduce the dissipation in Q2. Compensation for the preregulator is provided by C34 (3.3 nF) connected to the REGCOMP pin of the Si9122.

- **Boost:**
D1 (ES1B) and C8 (100 nF) provide the high-side drive "boost" (also known as "bootstrapping") function.
- **VM/CM Transition:**
R8 (4.7 k) and C13 (4.7 nF) control the transition from voltage mode to current mode control with frequency foldback, as outlined in the Si9122 data sheet.

Auxiliary Control Functions

A number of auxiliary control functions are implemented in order to provide required functionality.

These are:

- **On/Off Control:**
Pulling V_{INDET} to a voltage lower than 550 mV puts the converter into shutdown. This is done by driving the base of NPN transistor Q1 high. The switch SW1 is provided to connect the on-off pin to $+V_{\text{CC}}$ or to $-V_{\text{IN}}$ to do this. R89 (10 k) provides a measure of built-in pull-up or pull-down as required and can be overridden by a low-impedance source applied to the ON-OFF pin. 0 V (relative to $-V_{\text{IN}}$) will turn the converter on, while a 3.3 V to 12 V signal will turn the module off.
- **Overvoltage Detection:**
An overvoltage condition is detected on the output by comparing a divided version of the V_{OUT} with the reference voltage across ZD2. Upon detection of an overvoltage, comparator U7B drives a current through optocoupler diode U3B. The corresponding phototransistor in this device (U3A) is on the primary side. When U3A conducts, it turns on the PNP transistor Q10. The turn-on of Q10 causes Q9 to come

on, with R41 (100 k) providing a measure of noise margin. Q9 then pulls down on V_{INDET} , and also keeps Q10 on. Both of these functions are performed via dual diode D5. This results in the converter being latched in the "shutdown" state should an output overvoltage condition occur. To reset the latch formed by Q9 and Q10, the Eval Board's input power must be cycled. To avoid false trips at turn-on, R93 (10 k) and C39 (100 nF) provide a delay in the turn-on of Q10. This allows for the possibility of an indeterminate output condition on overvoltage comparator U7B at startup.

Resistors R38 and R39 form the voltage divider to the input of the overvoltage comparator, with C38 (100 nF) added to avoid false tripping under conditions of load transients or output noise. R39 is set at 1 k, and the resistor R38 is used to set the overvoltage trip point to nominally 10 % above the nominal output voltage level. The resulting table of values is given below:

Output Voltage (V)	3.3	2.5	1.8	1.5	1.225
Trip voltage (V)	3.63	2.75	1.98	1.65	1.35
R38 (k Ω)-to nearest 1 % value	1.96	1.24	0.619	0.340	0.100

R36 (1 M) works with R40 (4.7 k) and the Thevenin resistance of the divider chain to give approximately 30 mV of hysteresis.

- **Overtemperature Protection:**
This function is implemented with the LM56 programmable temperature controller, U5. The trip point is programmed using R42 (3.3 k) and R44 (18 k), (R43 is zero) for a value of approximately 107 $^{\circ}\text{C}$. The values of R42 and R44 may be changed if it is desired to operate with a higher limit point (typical of commercial converters). Typically a 2.2 k value can be used to give a value of 95 $^{\circ}\text{C}$ with 4.7 k corresponding to 115 $^{\circ}\text{C}$.
The LM56 requires a low value of supply current, which is derived from VCC via resistive divider R45 (2.2 k) and R46 (4.7 k). C40 (100 n) provides a measure of local supply decoupling. The temperature limiting function is effected by having an open-collector output of U5 pull down on the VINDET pin. C41 (100 n) bypasses the internal reference on U5.

Main Loop Control

Excellent transient response can be obtained from voltage mode controllers if a high crossover frequency is employed. In this converter design the output stage's LC

resonant peak occurs at about 13 KHz with no additional capacitive load, and placing the crossover frequency about 25 KHz is probably optimal. The controller design is typical of what is required for voltage-mode control loops with a phase boost branch (R25 and C48) used to achieve good phase margin (50 degrees) close to the gain crossover frequency. The controller operates by comparing the divided output voltage (R32 and R33/R34 are the divider chain) with the 1.225 V reference as obtained across ZD1.

The values of feedback loop components are designed for operation across the operating range of the converter.

R32 and R33/R34 are dependent on the output voltage programming as follows:

Output Voltage (V)	3.3	2.5	1.8	1.5	1.225
R32	1 k	1 k	1 k	1 k	0 Ω
R33	604 Ω	1 k	2.15	10 k	NF
R34	26.1 k	24.3 k	232 k	8.06 k	NF

The reference is fed from the local rail via R28 (10 k). R61 (10 k) and C33 (220 nF) assist in soft-start, causing a slow rise of the reference voltage when the converter begins operation. The rate of rise can be adjusted by changing the values of R61 and/or C33, and by adjusting the soft-start capacitor in the main controller. Control of the startup waveform is also enhanced by the use of the branch R31 (2.2 K) and C37 (470 nF).

U2, which is a high-speed optocoupler, is driven from the output of the error amplifier by R26 (680 Ω). The CTR of the optocoupler is in the range of 19 % to 50 % in the operating region, and thus sufficient current is available to develop the voltage required for full duty cycle control (0 to 1.65 V) across R7 (3.3 K), with noise pickup reduced by fitting C11 (270 pF).

Remote Sense Implementation

The controller works by setting the voltage between the positive and negative sense terminals. In some cases, where the converter is some distance from the load, the voltage drops across the supply leads or tracks can be excessive. In this case, the user may elect to connect separate leads or tracks back from the load to the converter. The resistors R29 and R30 (each 4.7 ohms) ensure that the lead connections do not "float" - in normal operation the sense pins are shorted to the respective output terminals. The local power return for the control circuit flows through R30 unless the negative sense pin is shorted to $-V_{OUT}$.

Caution - Do not attempt to pull current from the output sense pins, and do not short the sense pins to a pin of the opposite polarity.

Design Of Auxiliary Power Feed Arrangements

The converter is designed such that in normal operation voltages for operation of control and drive circuits are taken from the output inductor. In the "OFF" time for the input switches, the output synchronous rectifiers are on and the output voltage appears across the output inductor. It is thus relatively simple to put additional windings on the output inductor to get voltage levels consistent with powering the control and drive circuitry, with approximately 11 V - 13 V required at the input and approximately 6V required at the output. The rectifiers used are D8 on the input side and D13 on the output side, with resistors R47 and R16 (each 1ohm) serving to limit currents in these resistors under fault or transient conditions.

The windings on the output inductor need to be tapped so that the number of turns is appropriate to the output voltage. The tap is selected by stuffing one zero-ohm resistor out of a group of resistors for the input (R63, R64, R65, R68, R69) and the output (R70, R71, R72, R74, R75).

The following table shows the turns required, and the corresponding resistor to be stuffed, for the 6V secondary V_{CC} . All other resistor positions in this group must be open circuit.

Output Voltage (V)	3.3	2.5	1.8	1.5	1.225
Turns - Input	4	5	7	8	10
Turns - Output	2	3	4	5	6
0 Ω Resistor for Input	R69	R68	R65	R64	R63
0 Ω Resistor for Output	R71	R72	R75	R74	R70

When the output voltage is not available or is of insufficient magnitude, continuity of supply to the controller input circuitry is important. It is also important to ensure that under short-circuit conditions, supply is available to keep the output MOSFETs operating as synchronous rectifiers as otherwise body diode conduction can cause excessive dissipation. Another option here would be to run the converter in "hiccup mode", but this is not implemented in this design.

Linear regulators are thus provided at input and output to supply power to control and drive circuitry under such conditions.

The primary-side linear regulator is the Si9122 preregulator, as documented in the Si9122 datasheet. Q2 is used as an external pass transistor.

On the output side, any voltage on the drains of the FET rectifiers is peak-rectified by D4 and D6, with positions R57 and R78 provided to limit current if necessary (stuffed as 0 Ω). These diodes feed capacitors C28 and C29, with this circuitry also having a snubber and clamp function as discussed earlier. The voltage appearing across C28 and C29 is fed to a linear regulator Q89, with R56 (10 Ω) serving to limit dissipation in this device. The base of Q89 is held at a nominal voltage of 6.2 V by Zener diode ZD6, which is fed by resistor R58 (1.8 k). The result is that the voltage available at the emitter of Q89 is approximately 5.5 V, which is below the value derived from the output inductor winding. Therefore the linear regulator is not in operation under normal circumstances.

Dissipation in the linear regulators at input and output is greatly reduced by frequency foldback under conditions where they become relevant - under short circuit conditions the frequency is approximately one fifth of the normal set value, reducing drive current requirements of FET switches.

The voltage across C2 (470 nF) and C43 (1 μ F) is supplied to the gate drive circuitry. It is also fed via resistor R52 (270 Ω) to give a quasi-regulated supply across Zener diode ZD4 (4.3 V) for operation of control circuitry. R90 (3.3 k) is provided to discharge the capacitors to guarantee soft-start after a short interruption.

TEST POINTS

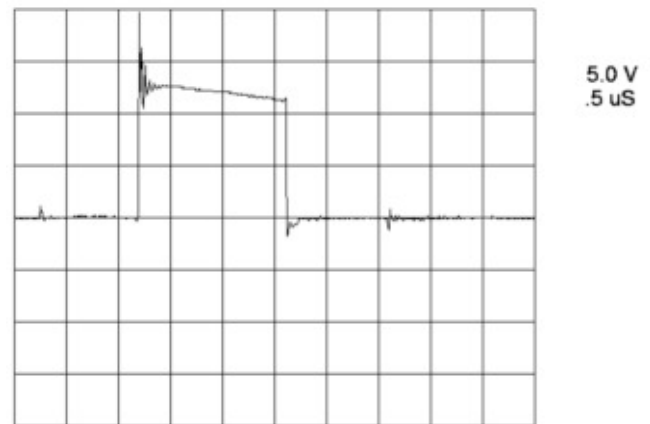
The board is equipped with numerous test points to facilitate user access to key nodes. These are of two types: small rectangles located primarily in the vicinity of the controller to allow access to signals at or near controller pins, and larger circles located in various positions to highlight key operating voltages.

The oscilloscope ground connection can be made to one of the appropriate input or output negative terminals for measurement of larger signal levels - some local ground connections are also available at locations throughout the board to facilitate measurements with shorter ground connections.

Inserting current probe loops on this Eval Board was not feasible, due to their inductance, resistance and size. However, measurement of the primary's low-side current can be made from the voltage derived across the current sense resistor, and an indication of secondary switch current can be obtained by measuring the voltage across the secondary-side MOSFETs. Resistor-diode combinations R73-D3 and R77-D7 are provided for this purpose. D3 and D7 clamp the maximum voltages at these points to one diode drop above ground during the "off" period of the synchronous rectifiers. This allows

oscilloscopic observation of the voltage during the conduction time of the synchronous rectifiers, where voltages on the order of tens of millivolts are of interest, without encountering dynamic range issues.

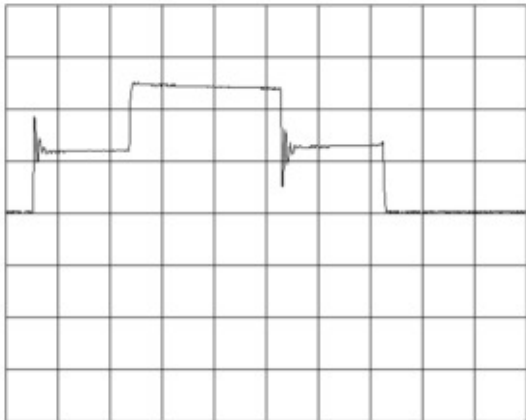
Waveforms at some key points in the circuit are shown below. Unless stated, these are with 48 V input, 3.3 V out, 30 A loading and without use of remote sensing.



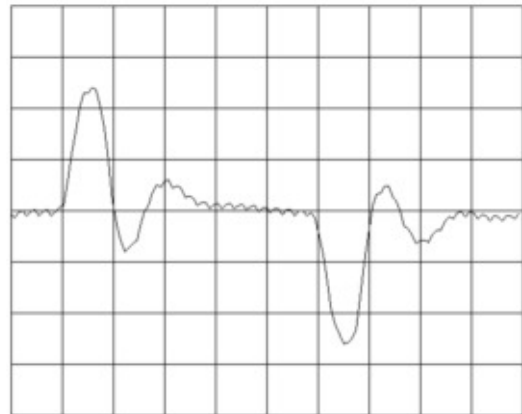
Secondary Side Synchronous Rectifier Drains - TP8 or TP11 measured with respect to ground (TP14).



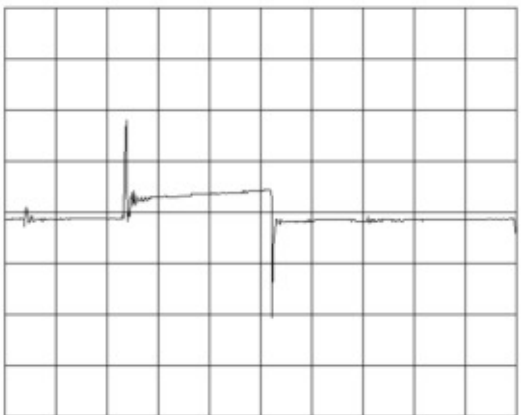
Resistor/Diode clamped Synchronous Rectifier Drains - TP21 or TP22 measured with respect to ground (TP14).



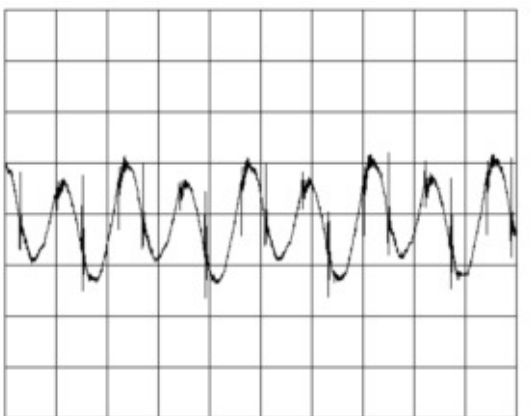
Primary switch node (LX, TP16) measured with respect to ground (TP25).



Output voltage response with 1A/ μ s transient from 15A to 30A, measured as for ripple-noise above.



Primary current sense voltage (TP18) measured with respect to ground (TP25).



Output ripple and noise measured across 10 μ F capacitor connected between +V_{OUT} and -V_{OUT} (20MHz oscilloscope bandwidth limit)

COMMENTS ON SPECIFICATIONS

Comments on some specifications normally applied to DC-DC converters, and how they are addressed with this implementation, are as follows:

Efficiency

The measured efficiency is approximately 90.5% at 3.3 V, 30 A output with a 48 V input. This reflects a total power loss of approximately 10.5 W, with approximately 2W of this in the transformer, 2 W in drive circuits and core losses, 1 W in primary FETs, 4 W in synchronous rectifiers and the balance in switching and snubber losses, body diode conduction and other areas. The efficiency can typically be increased by adding a further MOSFET in each of the input switching positions, and by adding a further MOSFET in each of the output switching positions.

When the converter is used at lower output voltages (1.8 V and below), it is possible to replace the Si7880ADP MOSFETs with 20 V-rated types such as the Si7886ADP. This device has an on-resistance approximately 35 % less than the 30 V-rated Si7880ADP, and use of three such devices in parallel can give very high efficiency for low output voltage applications.

Ripple and Noise

The converter is fitted with a number of ceramic capacitors, with a further grouping of polymer capacitors. This combination results in very low output ripple. If a somewhat higher figure is acceptable, then lower values of output capacitance (or capacitors with higher ESR) may be used.

Transient Response

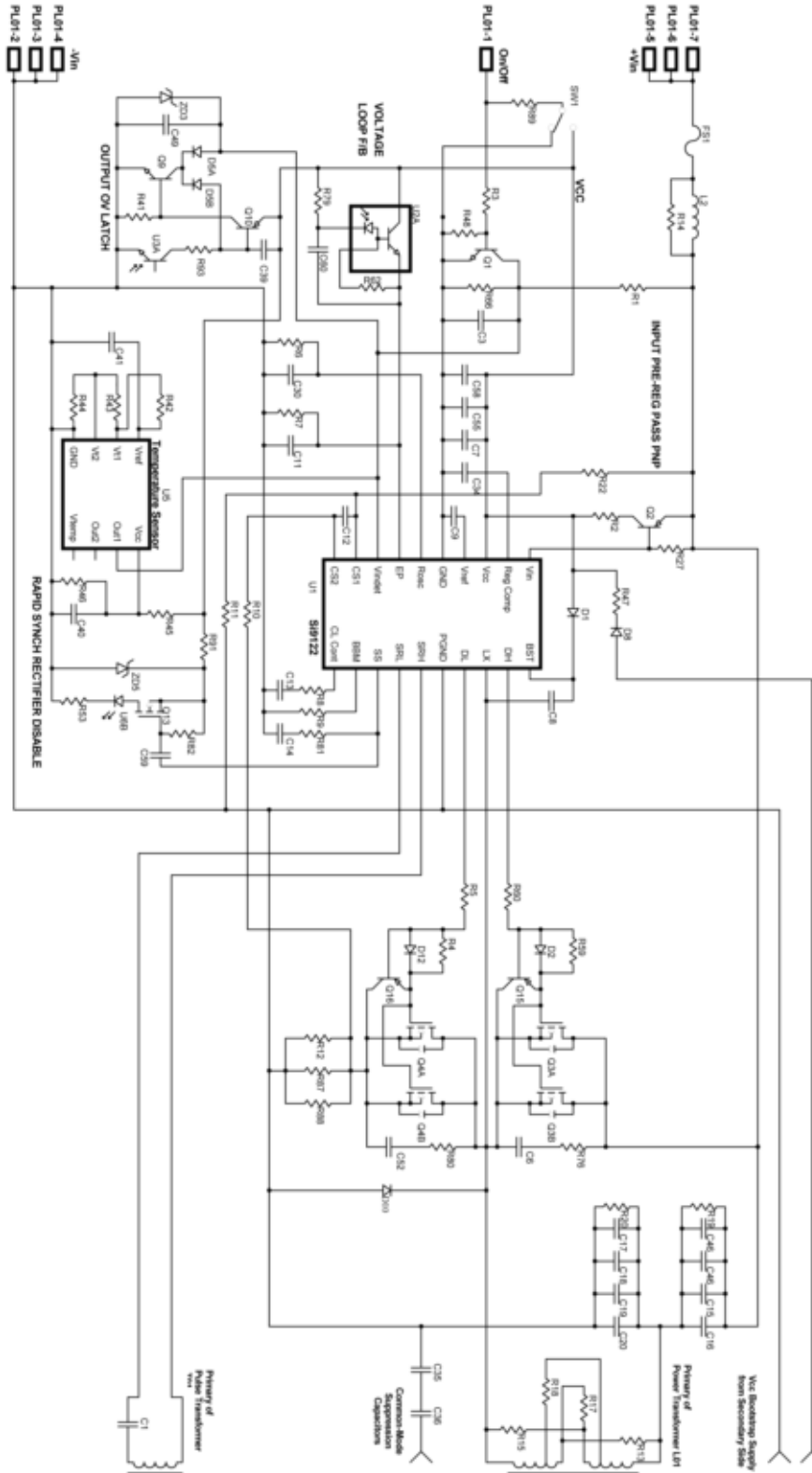
The load transient response of a voltage-mode converter operating with high efficiency and continuous conduction mode can be very good, if the crossover frequency is set appropriately. This requires the use of a feedback network designed to provide phase boost in the relevant part of the gain-phase curve so that adequate phase margin is obtained near the crossover frequency. To simplify the programming task between different voltage implementations, the feedback loop is designed to give acceptable performance across voltage settings from 1.225 V to 3.3 V.

SUMMARY

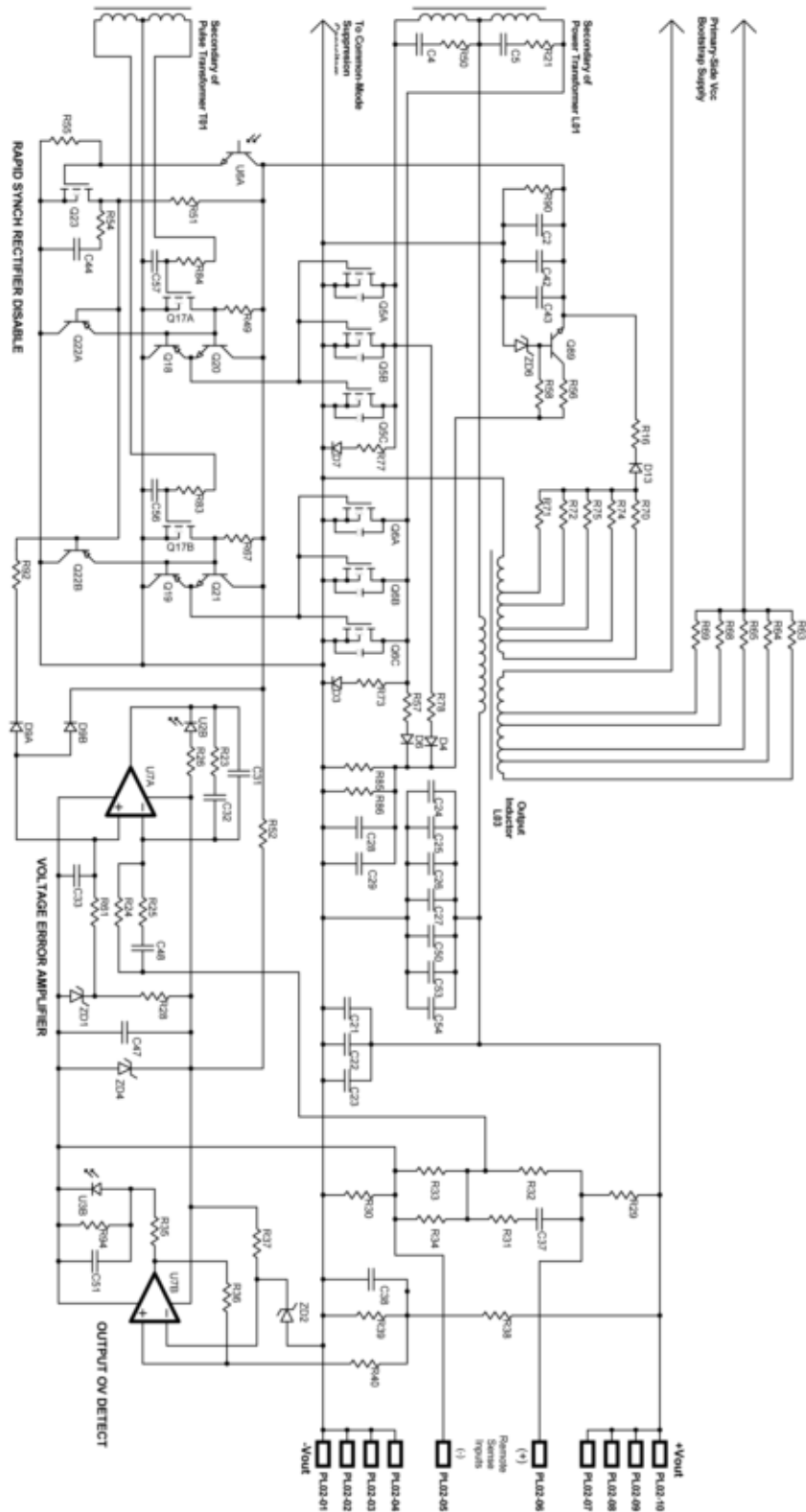
This Evaluation Board shows the capabilities of the Vishay Siliconix Si9122 controller IC in a typical application. Due to the number of test points and programming options provided on this Eval Board, and the desire to use no components smaller than 0603 case size, this board should not be considered a reference design. The objective has instead been to produce a flexible design that is consistent with current industry technique, yet with accessibility and flexibility such that such the user can test the performance of the Si9122 using this board, and can readily modify this board to test related converter designs based upon the Si9122.

SCHEMATICS AND COMPONENT MAPS

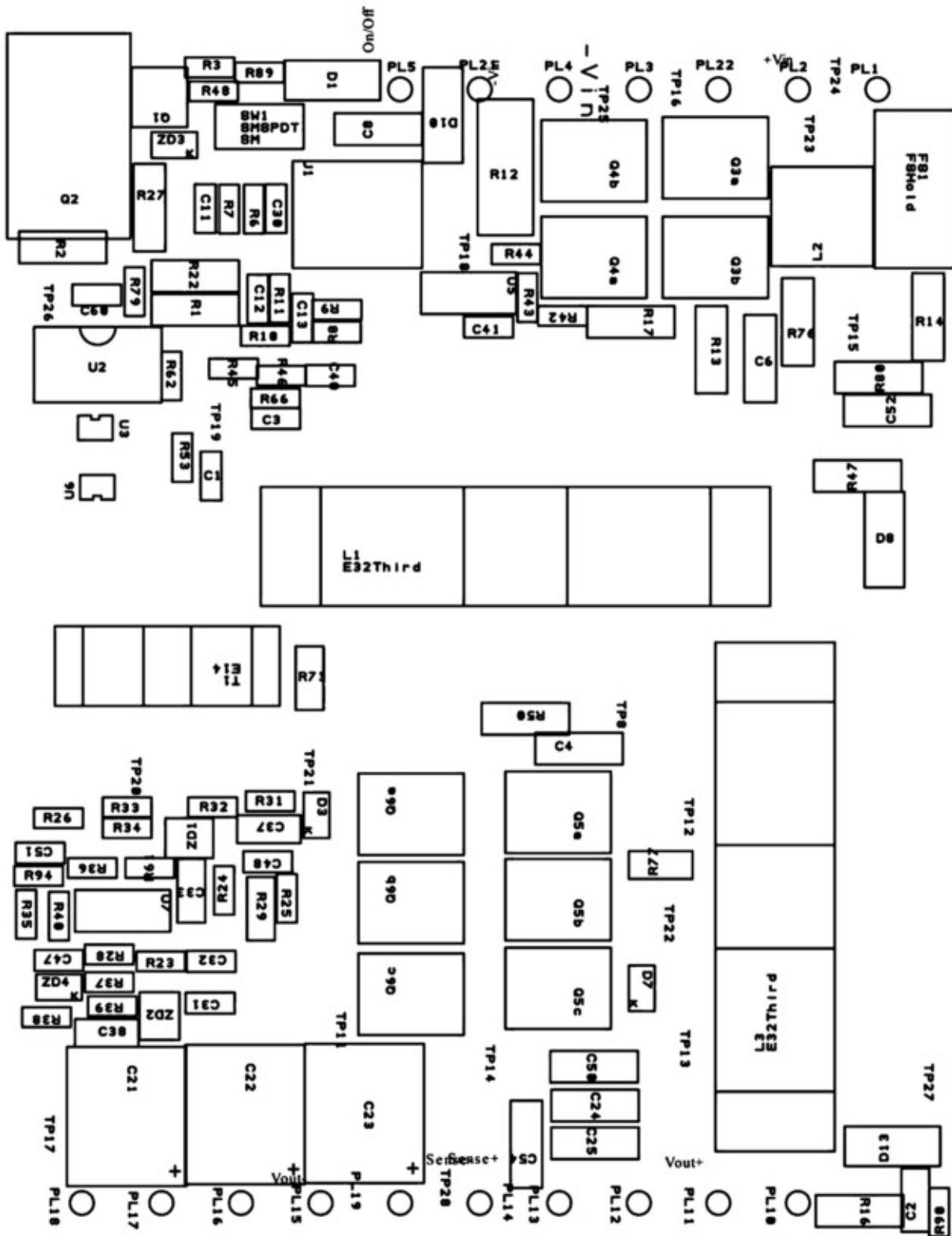
The schematics for the Si9122 Eval Board's primary-side and secondary-side circuitry are given below. Due to the extensive use of surface-mount devices, it is not practical to provide component identification markings on the board. Maps of top-side and bottom-side component positions are therefore provided on the two pages immediately following the schematics.



Si9122 Eval Board - Primary



Si9122 Eval Board - Secondary



Si9122 Eval Board Top-Side Component Map

Vishay Siliconix

BILL OF MATERIALS

The parts used on the Si9122 Eval Board are listed in the following Bill of Materials (BOM). Also shown in the BOM are those components that are not stuffed on this version of the Eval Board. Most parts that are not stuffed allow for changing output voltages and maximum currents, as described above.

Per Board	Reference Designator	Value and/or Type	Manufacturer	Manufacturer's Part #
5	C01, C38, C39, C40, C41	100 n X7R 0603 10 V 10 %	MuRata	GRM188R71E104KA01
3	C02, C37, C47	470 nF X7R 0805 16 V	MuRata	GRM21BR71C474KA01
2	C03, C49	1 nF X7R 0603 10 V	MuRata	GRM188R71H102KA01
2	C04, C05	10 n X7R 25V 1206	MuRata	GRM319R71H103KA01
2	C06, C52	470 pF X7R 1206 100 V	MuRata	GRM31M5C2D471JY21
1	C07	D-case Tant. 20 V 47 uF	Vishay	293D476X_020D2
2	C08, C09	100 nF X7R 1206 25 V	MuRata	GRM319R71E104KA01
2	C11, C30	220 pF X7R/C0G 0603 10 V	MuRata	GRM188R71H221KA01
3	C12, C56, C57	100 pF 0603 C0G 10 V 5 %	MuRata	GRM1885C1H101JA01
1	C13	4.7 nF X7R 0603 10 V	MuRata	GRM188R71H472KA01
3	C14, C51, C60	10 nF X7R 0603 10 V 10 %	MuRata	GRM188R71H103KA01
8	C15, C16, C17, C18, C19, C20, C45, C46	2.2 uF, 50 V, 1812 case	MuRata	GRM43ER71H225KA01
3	C21, C22, C23	150 uF Stacked Polymer, 6.3 V	Vishay	255D157X_6R3D2_045
7	C24, C25, C26, C27, C50, C53, C54	10 uF X7R 1206 6V3	MuRata	GRM31CR70J106KA01
2	C28, C29	220 nF X7R 1206 50 V	MuRata	GRM319R71H224KA01
2	C32, C48	2.2 nF X7R 0603 10 V	MuRata	GRM188R71H222KA01
1	C33	220 nF X7R 0805 10 V	MuRata	GRM21BR71C224KA01
1	C34	3.3 nF X7R 0603 10 V	MuRata	GRM188R71H332KA01
2	C35, C36	10 nF X7R 1812 1.5 KV	Johanson Dielectrics	152S43W103KV4
1	C43	1.0 uF X7R 1206 16 V	MuRata	GRM31MR71C105KA01
1	C58	2.2 uF X7R 1206 16 V	MuRata	GRM319R71C225KC11
1	C59	470 pF X7R 10 V 5 % 0603	MuRata	GRM188R71H471JA01
5	D01, D04, D06, D08, D13	1 A 100 V Ultrafast Rectifier	Vishay	ES1B
4	D02, D03, D07, D12	High Speed Signal Diode	Vishay	BAS16
1	D05	"BAV70 Dual Diode (Common Cathode)"	Vishay	BAV70
1	D09	"BAW56W Dual Diode (Common Anode)"	Diodes, Inc.	BAW56W
1	FS01 (Fuse Holder Type)	SMT Fuse Holder	Littelfuse	154005
N/A	FS01 (Fuse Type)	"5 A Fast-Blow Fuse (included with Littelfuse 154005)"	Littelfuse	454005
1	L01A	E32 Ferrite Core	Ferroxcube 3F3 Core (Customized part)	"Vishay Siliconix Core # 4100-000-024B"
1	L02	1.5 uH Filter Inductor	Vishay	IHLP2525CZ011R5
1	L03A	"Gapped E32 Ferrite Core (230 micron gap in center leg)"	Ferroxcube 3F3 Core (Customized part)	"Vishay Siliconix Core # 4100-000-027B"
2	L01B, L03B	PLT32 Ferrite Core	Ferroxcube 3F3 Core (Customized part)	"Vishay Siliconix Core # 4100-000-028B"
1	PCB	Si9122 EVB PCB	Custom PCB for Vishay Siliconix	Si9122 EVB PCB
1	PL01	7 x 1 header, 0.2" pitch	Samtec	FWS-07-01-T-S
1	PL02	10 x 1 header, 0.2" pitch	Samtec	FWS-10-01-T-S
2	Q01, Q09	SOT-23 NPN Transistor with Integrated Resistors (2 x 22 k)	Panasonic	UNR221200L



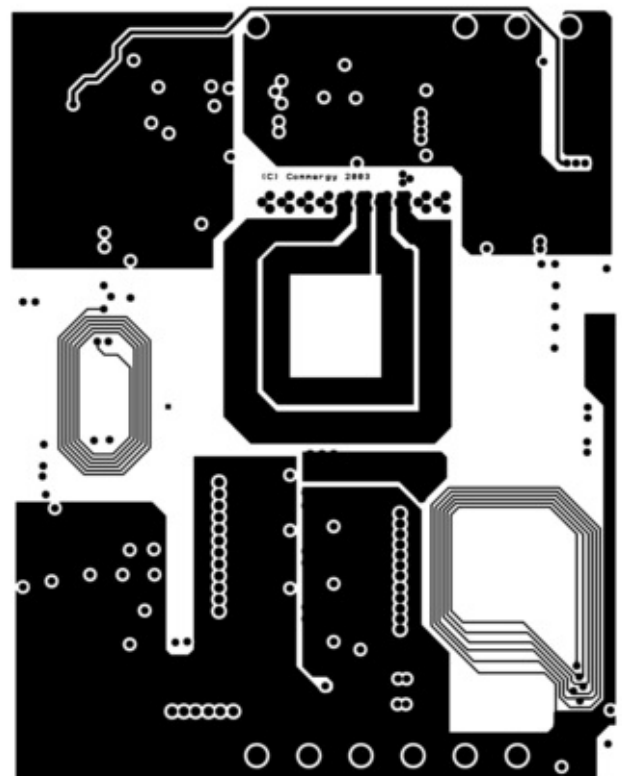
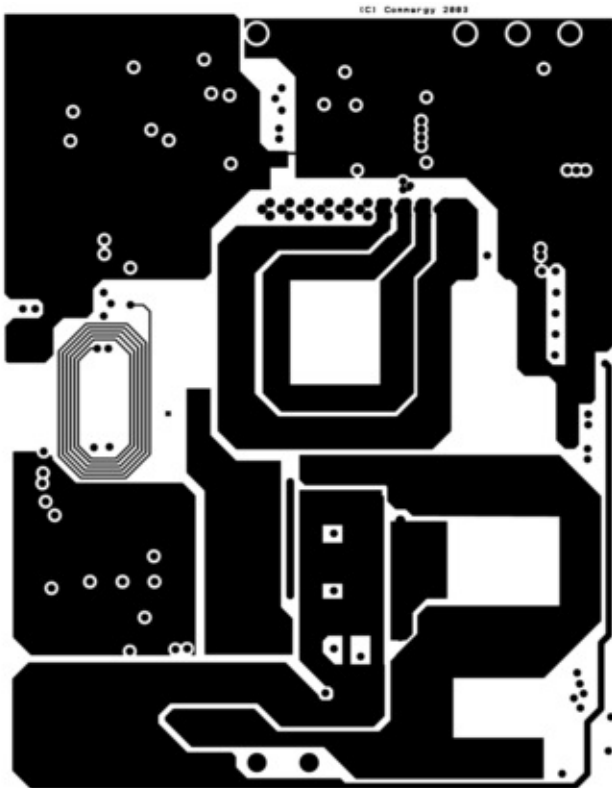
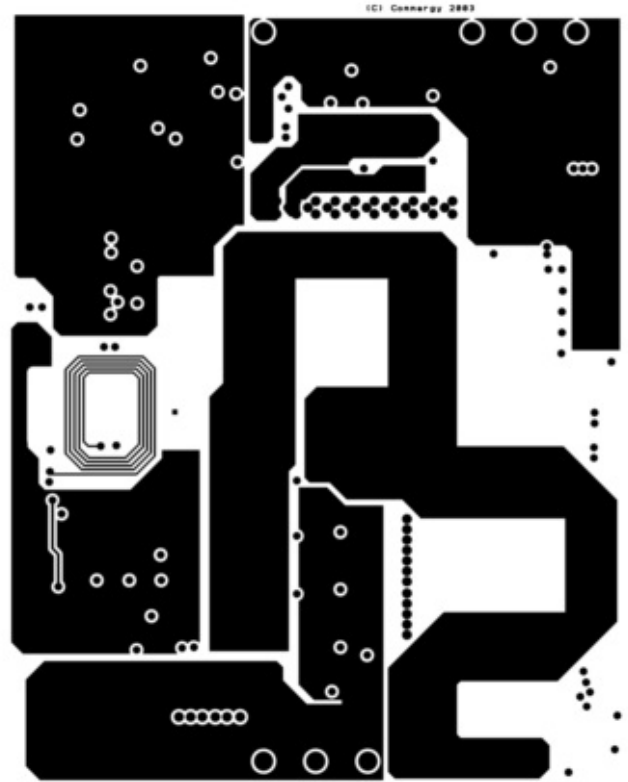
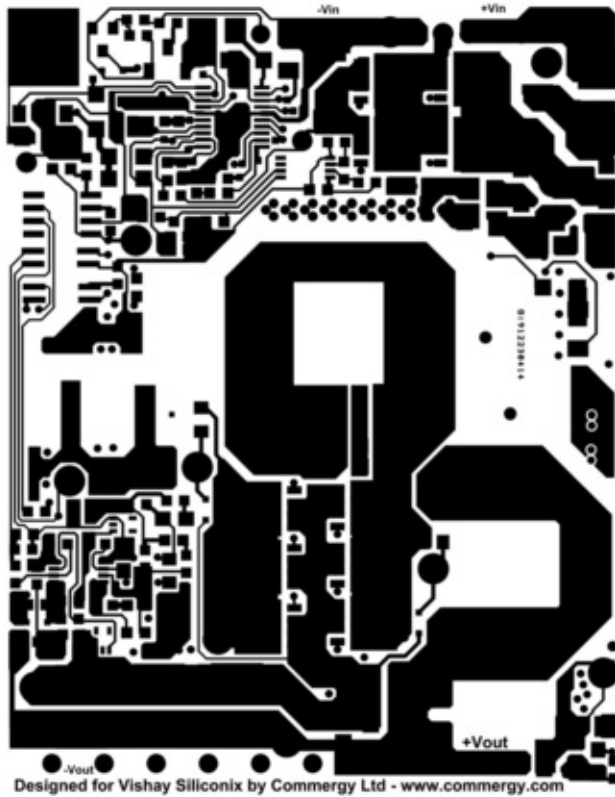
Per Board	Reference Designator	Value and/or Type	Manufacturer	Manufacturer's Part #
1	Q02	PNP Transistor, 100 V, DPAK	On Semi	MJD32C
2	Q03A, Q04A	PowerPAK SO-8 MOSFET	Vishay	Si7456DP
6	Q05A, Q05B, Q05C, Q06A, Q06B, Q06C	PowerPAK SO-8 MOSFET	Vishay	Si7880ADP
1	Q10	SOT-23 PNP Transistor with Integrated Resistors (2 x 47 k)	Panasonic	UNR211300L
1	Q13	P-Channel MOSFET, SOT-23	Vishay	TP0610K
4	Q15, Q16, Q18, Q19	High Current PNP, SOT-23	Zetex	FMMT717
1	Q17	Si1900DL	Vishay	Si1900DL
2	Q20, Q21	High Current NPN, SOT-23	Zetex	FMMT617
1	Q22	NPN Signal Transistor, SOT-363	Diodes, Inc.	MMDT2907A
1	Q23	N-Channel MOSFET, SOT-23	Philips	BSN20
1	Q89	NPN Transistor, 80 V, DPAK	On Semi	MJD44H11
1	R01	90.9 K 1206 1 %	Vishay	CRCW12069092F
5	R02, R13, R15, R57, R78	0R0 1206 Jumper	Vishay	CRCW1206000Z
1	R03	47K 0603 5 %	Vishay	CRCW0603473J
1	R05	11R 0805 5 %	Vishay	CRCW080511RJ
1	R06	39K2 0603 1 %	Vishay	CRCW06033922F
3	R07, R90, R91	3K3 0603 5 %	Vishay	CRCW0603332J
4	R08, R40, R53, R55	4K7 0603 5 %	Vishay	CRCW0603472J
1	R09	27K 0603 5 %	Vishay	CRCW0603273J
2	R10, R11	330R 0603 1 %	Vishay	CRCW0603330RF
1	R12	0.015 Ω 1 % WSL 2512	Vishay	WSL2512 0.015W \pm 1.0%
1	R14	4R7 1206 5 %	Vishay	CRCW12064R7J
3	R16, R21, R50	1R0 1206 5 %	Vishay	CRCW12061R0J
2	R19, R20	100K 1206 1 %	Vishay	CRCW1003F
1	R22	1.5 Meg 1206 5 %	Vishay	CRCW1206155J
1	R23	1K5 0603 5 %	Vishay	CRCW0603152J
7	R24, R28, R35, R61, R81, R89, R93	10K 0603 5 %	Vishay	CRCW0603103J
4	R25, R43, R68, R72	0R0 0603 Jumper	Vishay	CRCW0603000Z
1	R26	680R 0603 5 %	Vishay	CRCW0603680RF
1	R27	1.0 Meg 1206 5 %	Vishay	CRCW1206105J
2	R29, R30	4R7 0805 5 %	Vishay	CRCW08054R7J
2	R31, R45	2K2 0603 5 %	Vishay	CRCW0603222J
3	R32, R33, R39	1K0 0603 1 %	Vishay	CRCW06031001F
1	R34	24K3 0603 1 %	Vishay	CRCW06032432F
2	R36, R82	1.0 Meg 0603 5 %	Vishay	CRCW0603105J
2	R37, R66	10K 0603 1 %	Vishay	CRCW06031002F
1	R38	1K24 0603 1 %	Vishay	CRCW06031241F
1	R41	100K 0603 5 %	Vishay	CRCW0603104J
1	R42	3K3 0603 1 %	Vishay	CRCW06033301F
1	R44	18K 0603 1 %	Vishay	CRCW06031802F
1	R46	4K7 0603 1 %	Vishay	CRCW06034701F
1	R47	22R 1206 5 %	Vishay	CRCW120622RF
2	R49, R67	270R 0805 5 %	Vishay	CRCW0805270RJ
1	R52	270R 0603 5 %	Vishay	CRCW0603270RJ
1	R56	10R 1206 5 %	Vishay	CRCW120610RJ
1	R58	1K8 1206 5 %	Vishay	CRCW1206183J
1	R60	11R 0805 5 %	Vishay	CRCW080511RJ
2	R73, R77	3K3 0805 5 %	Vishay	CRCW0805332J
2	R76, R80	22R 1206 5 %	Vishay	CRCW120622RJ
1	R79	82K 0603 5 %	Vishay	CRCW0603823J
2	R83, R84	100R 0603 5 %	Vishay	CRCW0603100RJ

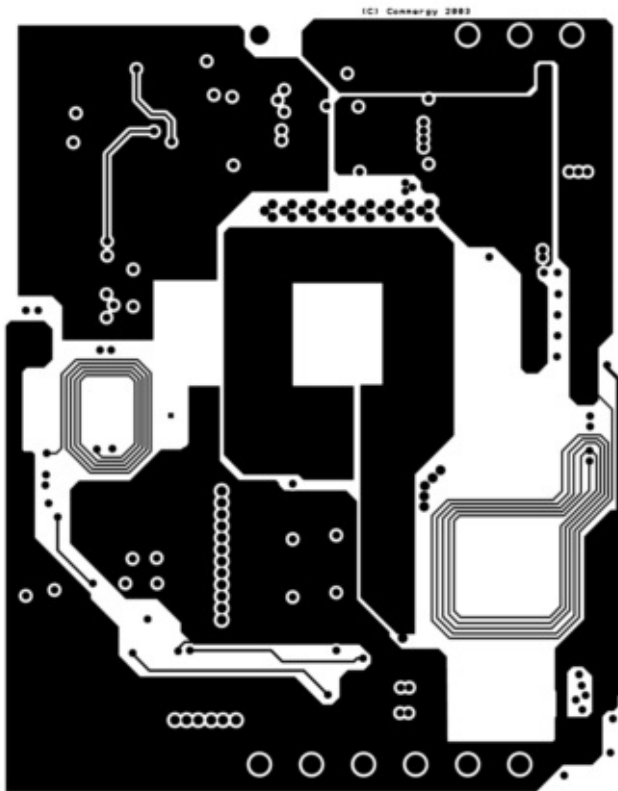


Per Board	Reference Designator	Value and/or Type	Manufacturer	Manufacturer's Part #
2	R85, R86	3K3 1206 5 %	Vishay	CRCW1206332J
1	R87	0.015 Ω 1 % WSL 1206	Vishay	WSL1206 0.015W \pm 1.0%
1	R92	10R 0603 5 %	Vishay	CRCW060310RJ
1	R94	22K 0603 5 %	Vishay	CRCW0603223J
1	SW01	SPDT Switch	Vishay (BC Components)	CAS120A1
1	T01A	E14/3.5/5-3F3 Ferrite Core	Ferroxcube	3F3 E-Core
1	T01B	PLT14/5/1.5-3F3 Ferrite Core	Ferroxcube	3F3 Plate Core
1	U01	SMPS Controller IC	Vishay	Si9122DQ
1	U02	High Speed Optocoupler	Vishay	SFH6316T
2	U03, U06	Optocoupler	Vishay	TCMT1103
1	U05	Temperature Sensor IC	National Semi	LM56CIMM
1	U07	Dual Op Amp	National Semi	LMV358MM
2	ZD01, ZD02	Precision Shunt Regulator	National Semi	LM4041CIM7-1.2
2	ZD03, ZD05	6V8 Zener 5 mA	Vishay	GDZ6.8B
1	ZD04	4V3 Zener 5 mA	Vishay	GDZ4.3B
1	ZD06	6V2 Zener 5 mA	Vishay	GDZ6.2B
NOT STUFFED / UNUSED DESIGNATORS:				
0	C31, C42, C44, C55	Not Stuffed		
0	D10	Not Stuffed		
0	Q03B, Q04B	Not Stuffed		
0	R04, R17, R18, R48, R51, R54, R59, R62, R63, R64, R65, R69, R70, R71, R75, R74, R88	Not Stuffed		
0	C10	Unused Designator(s)		
0	D11	Unused Designator(s)		
0	Q07, Q08, Q11, Q12, Q24 – Q88	Unused Designator(s)		
0	U04	Unused Designator(s)		

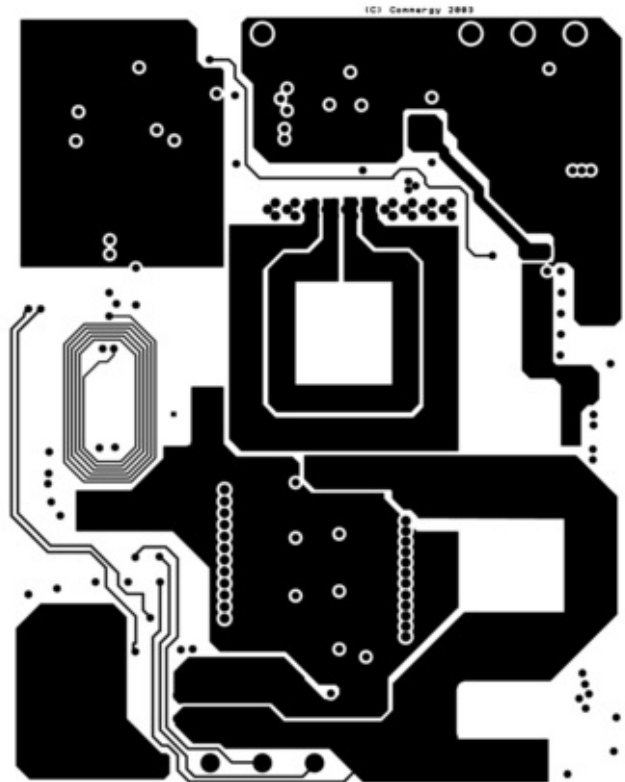
ARTWORK FOR THE PRINTED CIRCUIT BOARD

For any DC-to-DC converter, the artwork is of interest to show proper layout of the power and signal paths surrounding the controller IC. In a design using embedded planar magnetics, having the artwork is even more important, as the magnetics require a multi-layer PCB. There will therefore be both signal and power traces in the layers between the traditional "top" and "bottom" sides of the board. The artwork for the 10 layers of the Si9122 Eval Board is therefore given on the following 10 pages.

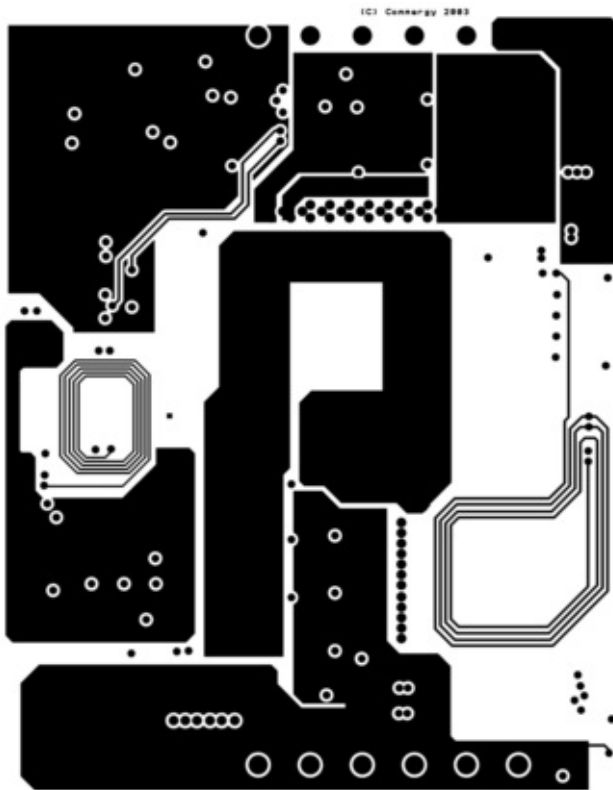




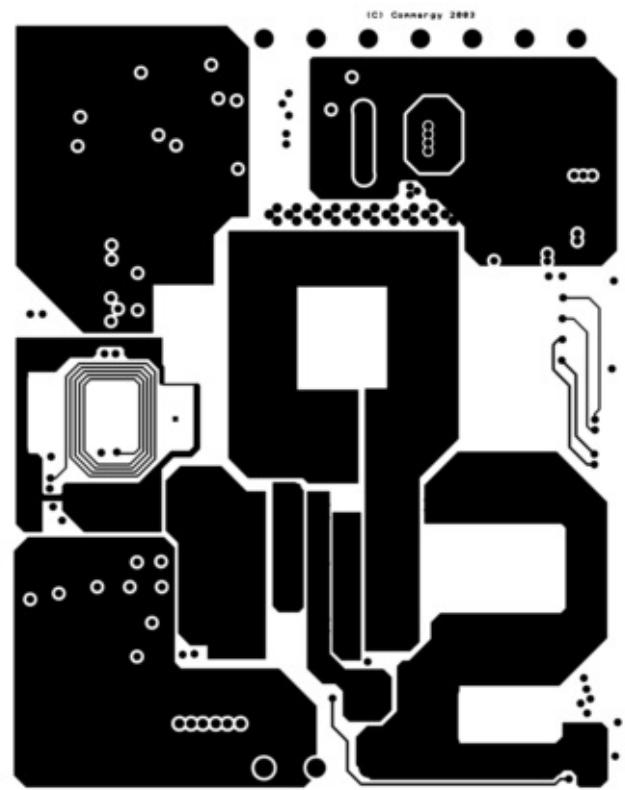
PCB LAYER #5



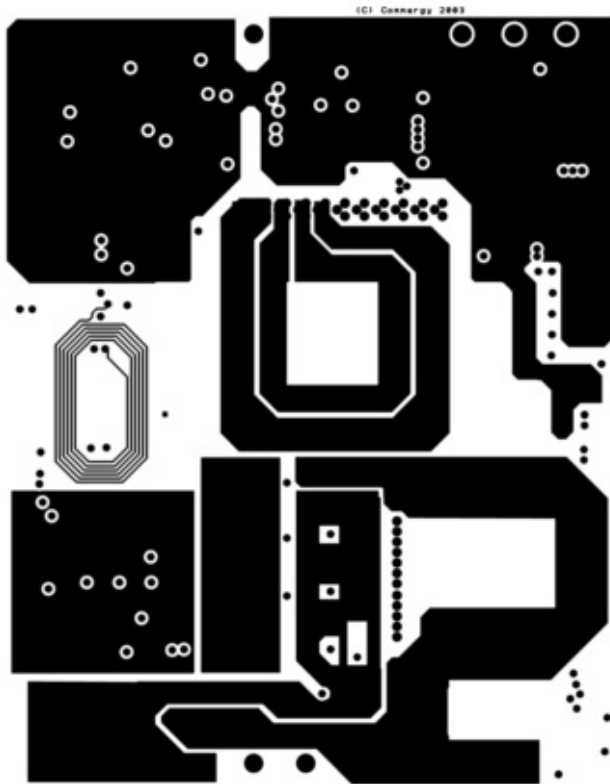
PCB LAYER #7



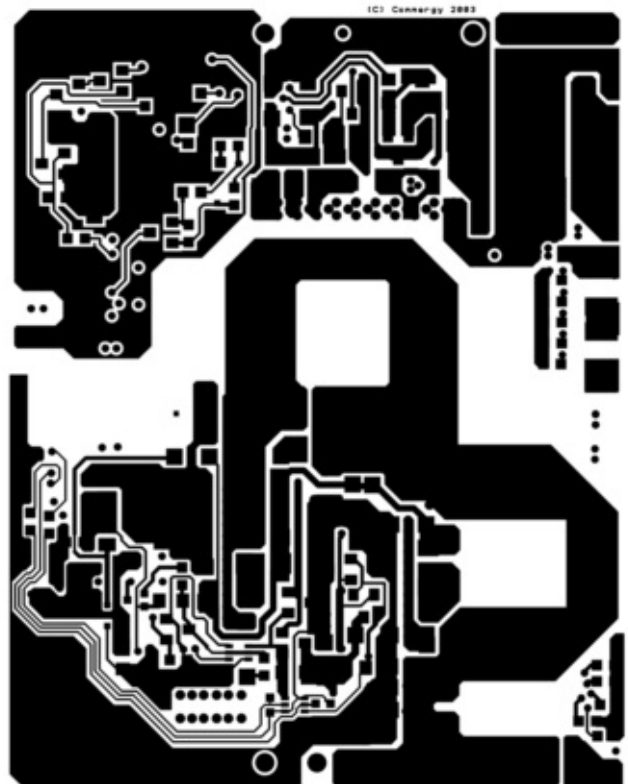
PCB LAYER #6



PCB LAYER #8



PCB LAYER #9



PCB LAYER #10 ("BOTTOM" LAYER)



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