

# N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A) <sup>d</sup> Q <sub>g</sub> (Typ.				
60	0.036 at V <sub>GS</sub> = 10 V	8	10.5 nC			
00	0.043 at V <sub>GS</sub> = 4.5 V	8	10.5110			

#### **FEATURES**

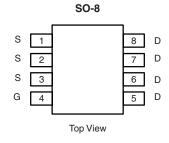
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Optimized for "Low Side" Synchronous Rectifier Operation
- 100 % R<sub>g</sub> and UIS Tested





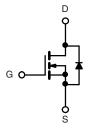
#### **APPLICATIONS**

CCFL Inverter



Ordering Information: Si4436DY-T1-E3 (Lead (Pb)-free)

Si4436DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_{A}$	= 25 °C, unless other	erwise noted		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v
	T <sub>C</sub> = 25 °C		8 <sup>a</sup>	
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	1 .	6.8	
Continuous Diam Current (1) = 130 C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	6.1 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		4.8 <sup>b, c</sup>	^
Pulsed Drain Current	I <sub>DM</sub>	25	A	
Continuous Course Prain Diade Current	T <sub>C</sub> = 25 °C	I.	4.2	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	ls –	2.1 <sup>b, c</sup>	
Avalanche Current	. 0.4	I <sub>AS</sub>	15	
Single-Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	11.2	mJ
	T <sub>C</sub> = 25 °C		5	
Mavinovna Davier Dissipation	T <sub>C</sub> = 70 °C		3.2	w
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>b, c</sup>	VV
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	38	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	20	25	C/ <b>VV</b>	

#### Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. Maximum under Steady State conditions is 85  $^{\circ}\text{C/W}.$

# **Si4436DY**

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	-				1		
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		55		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 6.3			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.5		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Dvain Current	1	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	1		1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			Α	
D : 0	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.6 A		0.030	0.036	.0.	
Drain-Source On-State Resistance <sup>a</sup>	H <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 4.2 \text{ A}$		0.035	0.043		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 4.6 A		20		S	
Dynamic <sup>b</sup>				•	•		
Input Capacitance	C <sub>iss</sub>			1100		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		90			
Reverse Transfer Capacitance	C <sub>rss</sub>			55			
Total Cata Charge	0	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 4.6 \text{ A}$		21	32	nC	
Total Gate Charge	Q <sub>g</sub>			10.5	16		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 4.6 \text{ A}$		3.5			
Gate-Drain Charge	Q <sub>gd</sub>			4.2			
Gate Resistance	$R_g$	f = 1 MHz		3.3	5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			20	30		
Rise Time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, R_{L} = 5.4 \Omega$		150	225		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 5.6 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t <sub>f</sub>			60	90	no	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 30 V, $R_L$ = 5.4 $\Omega$		15	25		
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong 5.6 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	40		
Fall Time	t <sub>f</sub>			10	15		
<b>Drain-Source Body Diode Characterist</b>	ics						
Continous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			4.2	۸	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				25	Α	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 2 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			25	50	ns	
dy Diode Reverse Recovery Charge O				25	50	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 5.5 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		19		nc	
Reverse Recovery Rise Time	t <sub>b</sub>			6		ns	

#### Notes:

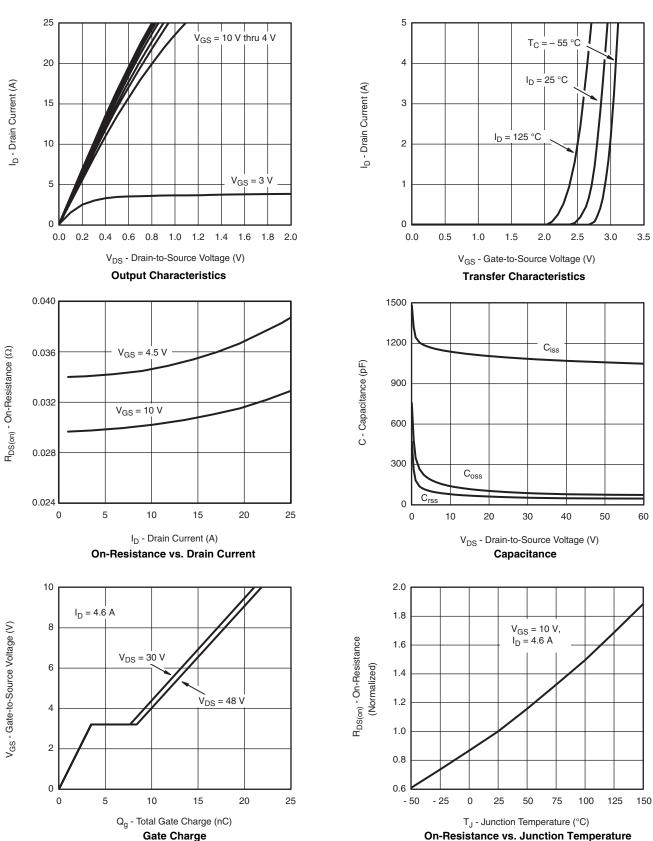
- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

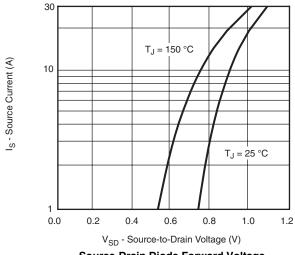


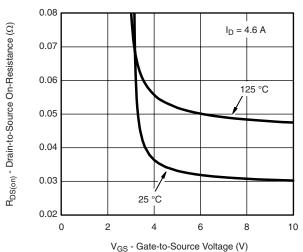
# **Si4436DY**

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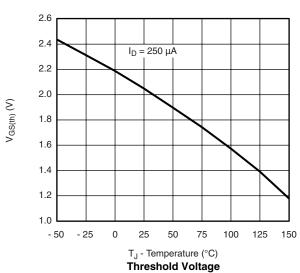
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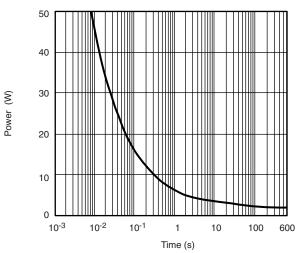




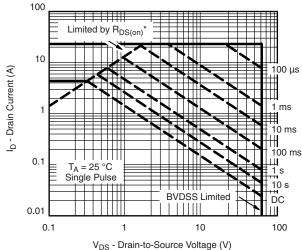
#### Source-Drain Diode Forward Voltage







Single Pulse Power, Junction-to-Ambient



V<sub>DS</sub> - Drain-to-Source Voltage (V)

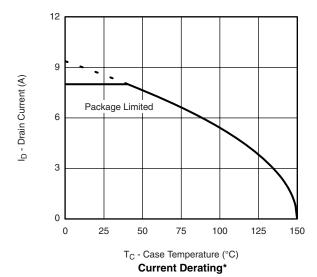
\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

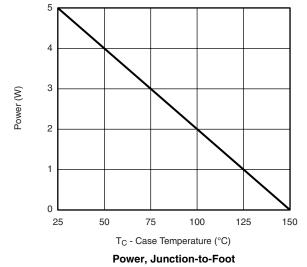
Safe Operating Area



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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





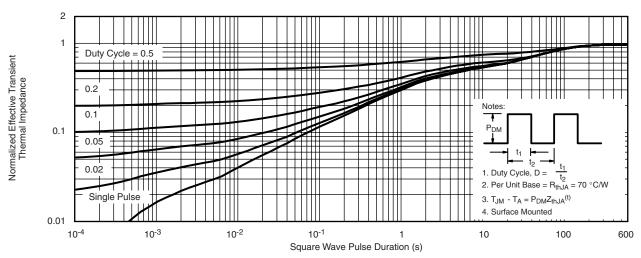
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

# **Si4436DY**

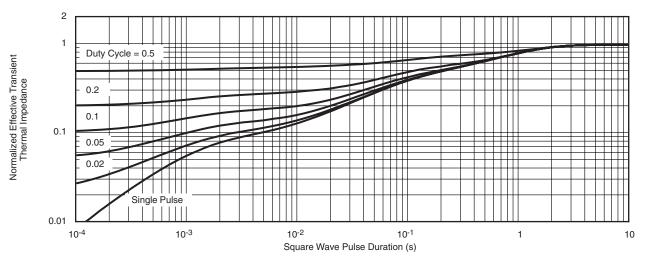
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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg273664">www.vishay.com/ppg273664</a>.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	MILLIMETERS INCHES				
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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