

## P-Channel 20-V (D-S) MOSFET

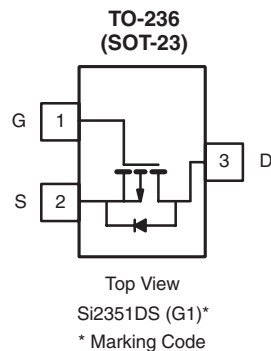
MOSFET PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 20	0.115 at $V_{GS} = - 4.5$ V	- 3.0	3.2 nC
	0.205 at $V_{GS} = - 2.5$ V	- 2.2	

### FEATURES

- Halogen-free Option Available
- TrenchFET<sup>®</sup> Power MOSFET
- PWM Optimized
- 100 %  $R_g$  Tested



**RoHS**  
COMPLIANT



Ordering Information: Si2351DS-T1-E3 (Lead (Pb)-free)  
Si2351DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	- 2.8
		$T_C = 70$ °C	- 2.4
		$T_A = 25$ °C	- 2.2 <sup>b, c</sup>
		$T_A = 70$ °C	- 1.8 <sup>b, c</sup>
Pulsed Drain Current	$I_{DM}$	- 10	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	- 0.9 <sup>1b, c</sup>
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	2.1
		$T_C = 70$ °C	1.5
		$T_A = 25$ °C	1.0 <sup>b, c</sup>
		$T_A = 70$ °C	0.7 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$R_{thJA}$	90	115	°C/W
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	60	75	

Notes:

- Based on  $T_C = 25$  °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- Maximum under Steady State conditions is 130 °C/W.

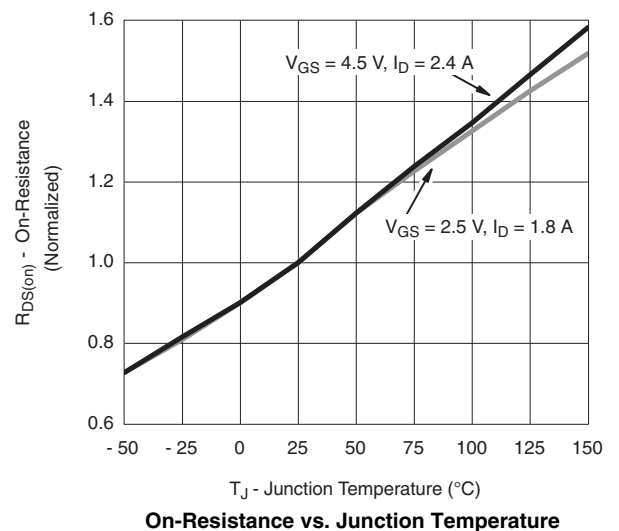
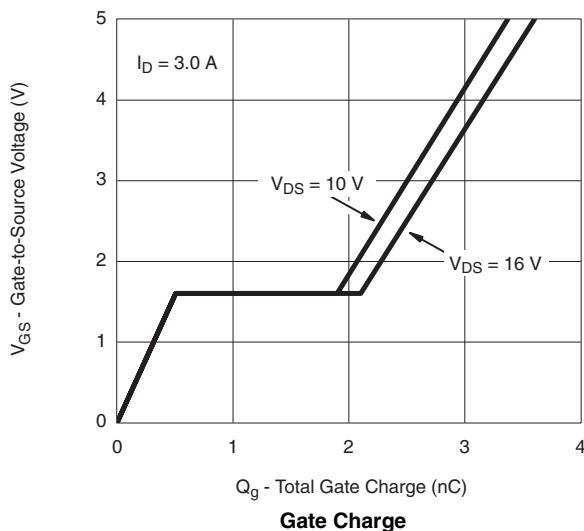
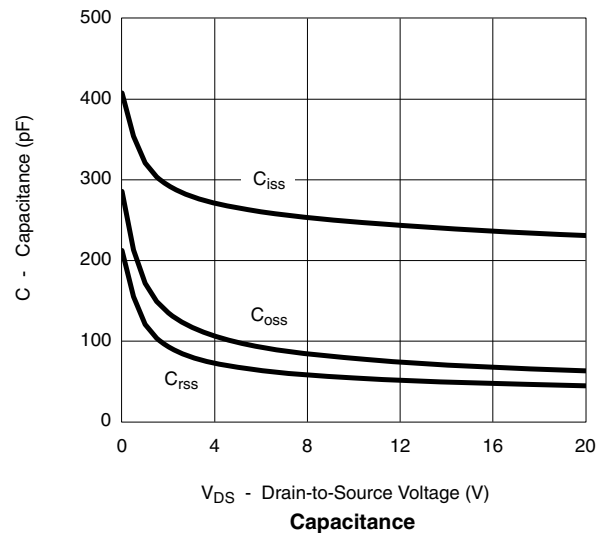
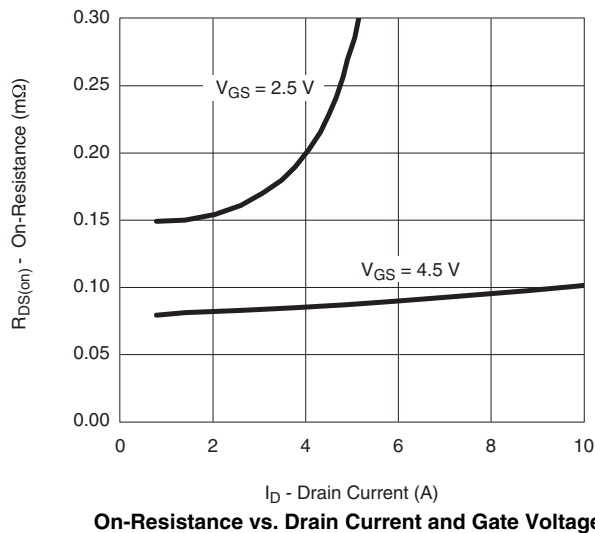
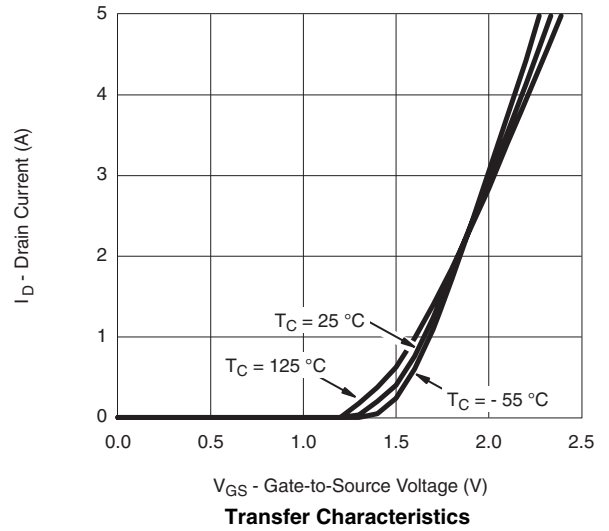
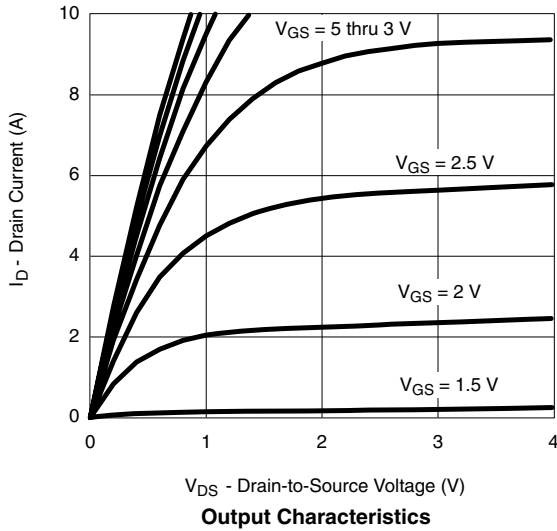
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{DS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-16.7		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.6		-1.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.4\text{ A}$		0.092	0.115	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -1.8\text{ A}$		0.164	0.205	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -2.4\text{ A}$		5.5		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		250		pF
Output Capacitance	$C_{oss}$			80		
Reverse Transfer Capacitance	$C_{rss}$			55		
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -5.0\text{ V}, I_D = -2.4\text{ A}$		3.4	5.1	nC
				3.2	5	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -2.4\text{ A}$		0.5		
Gate-Drain Charge	$Q_{gd}$			1.4		
Gate Resistance	$R_g$		$f = 1\text{ MHz}$		8.5	13
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 5.26\text{ }\Omega$ $I_D \cong -1.9\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 1\text{ }\Omega$		9	14	ns
Rise Time	$t_r$			30	45	
Turn-Off Delay Time	$t_{d(off)}$			32	48	
Fall Time	$t_f$			16	24	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-2.0	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				-10	
Body Diode Voltage	$V_{SD}$	$I_S = -2.0\text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		17	26	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			5	8	nC
Reverse Recovery Fall Time	$t_a$			14		ns
Reverse Recovery Rise Time	$t_b$			3		

Notes:

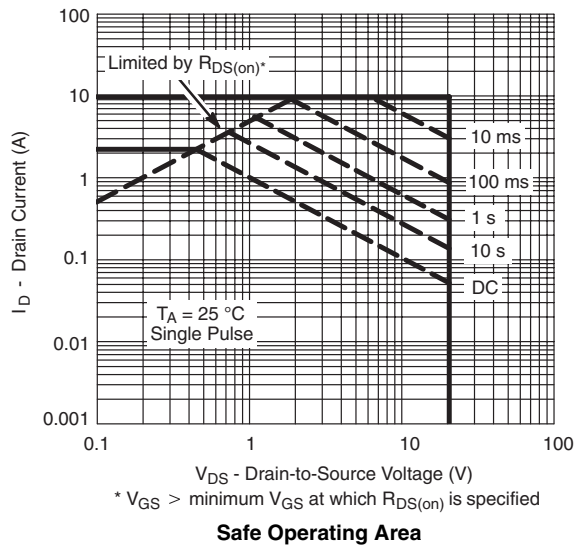
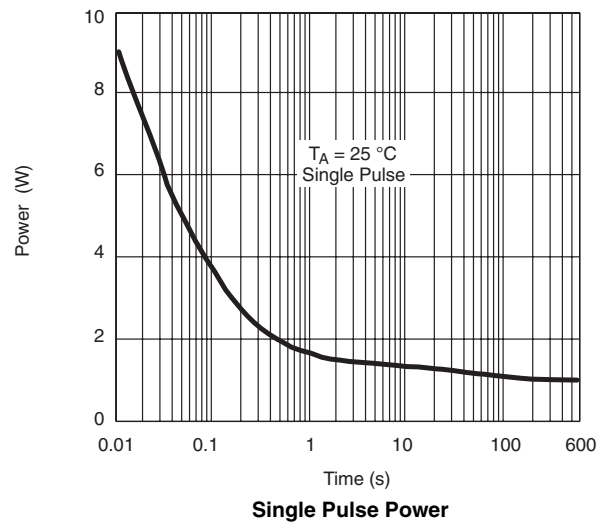
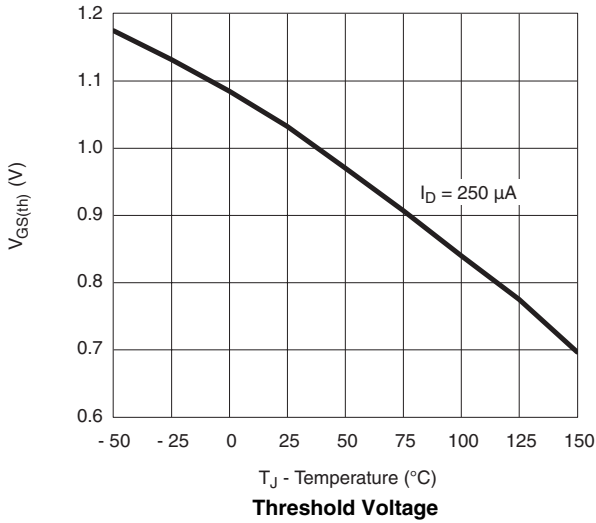
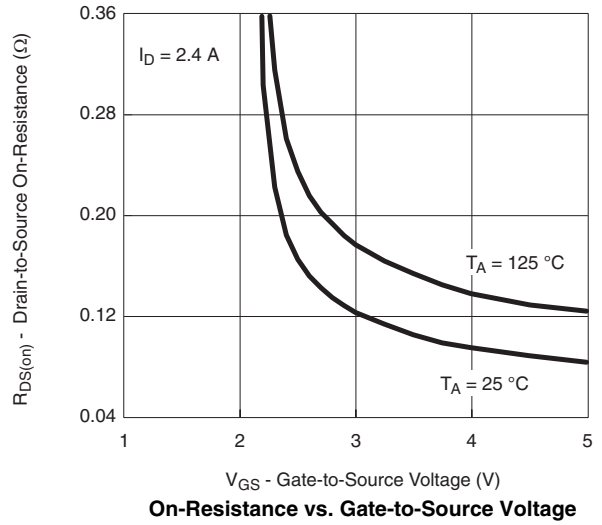
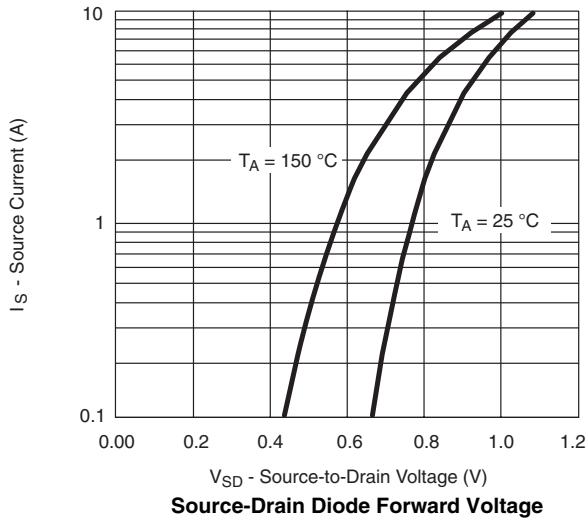
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

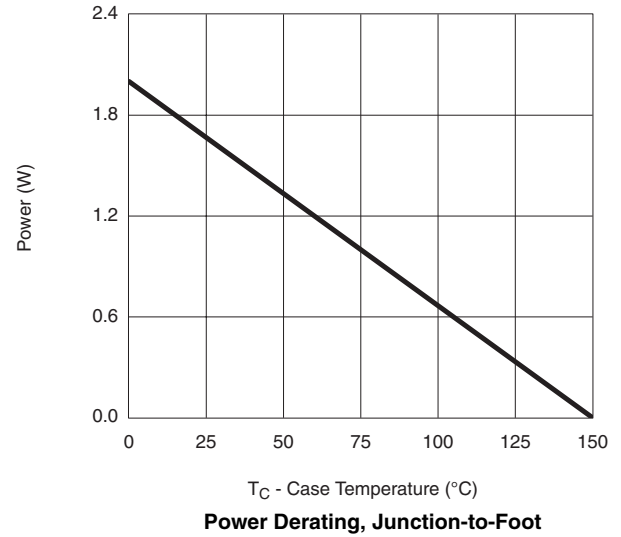
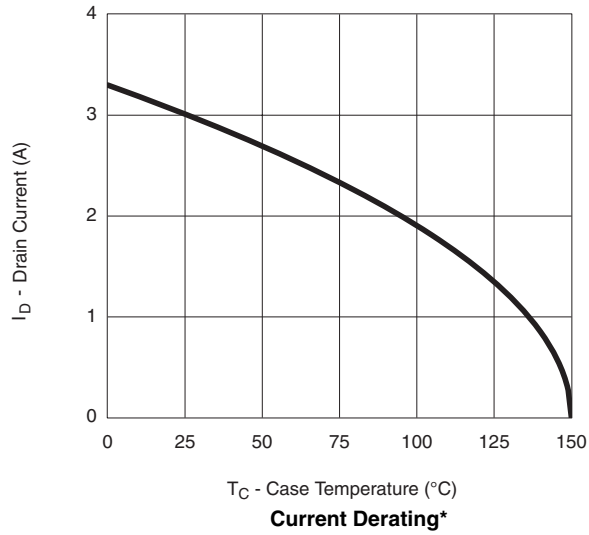
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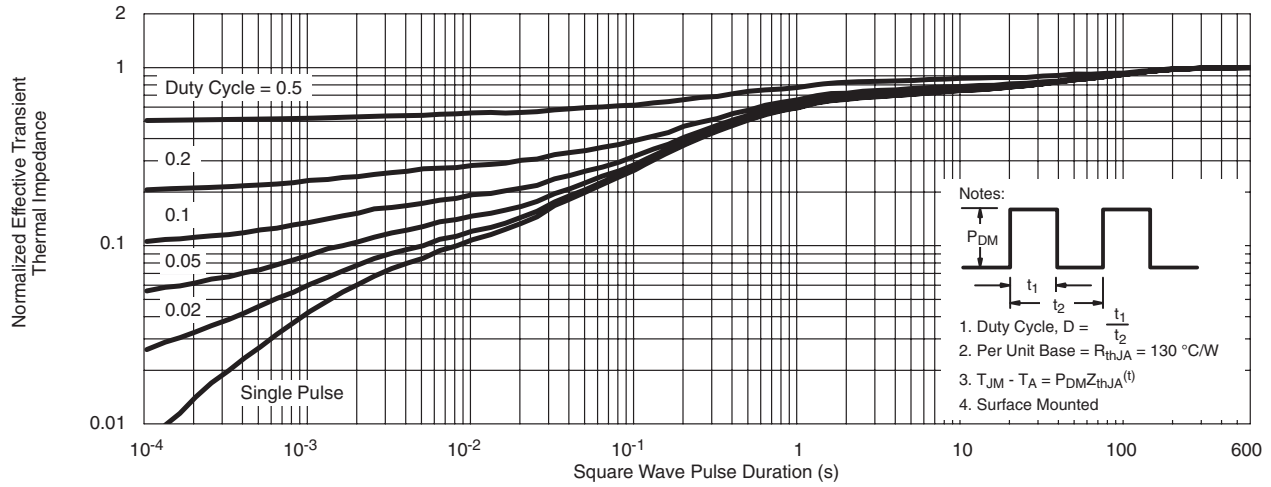


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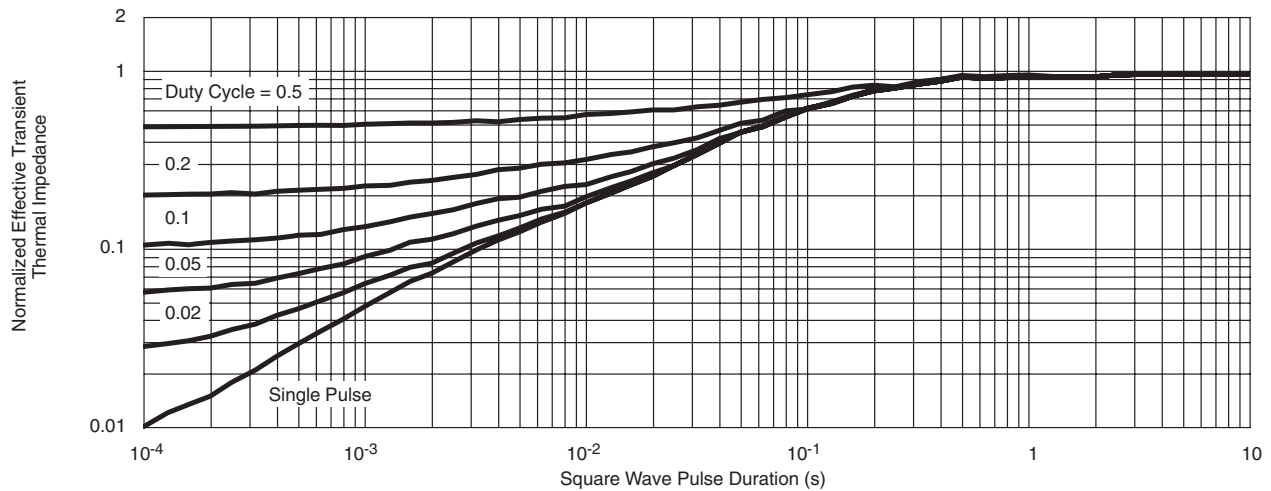


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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