N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
20	0.015 at V_{GS} = 4.5 V	12	21 nC
	0.017 at V_{GS} = 2.5 V	12	
	0.021 at V_{GS} = 1.8 V	12	

FEATURES

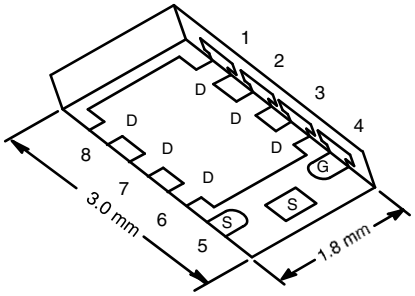
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.8 mm Profile
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT

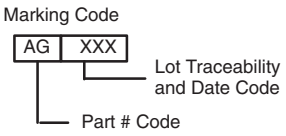
APPLICATIONS

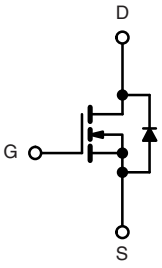
- Load Switch, PA Switch, and for Portable Applications
- Point-of-Load

PowerPAK ChipFET Single



Bottom View





N-Channel MOSFET

Ordering Information:
Si5486DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	12[a]	A
	T_C = 70 °C		12[a]	
	T_A = 25 °C		11.6[b, c]	
	T_A = 70 °C		9.3[b, c]	
Pulsed Drain Current		I_{DM}	40	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	12[a]	
	T_A = 25 °C		2.6[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	31	W
	T_C = 70 °C		20	
	T_A = 25 °C		3.1[b, c]	
	T_A = 70 °C		2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	34	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3	4	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 90 °C/W.

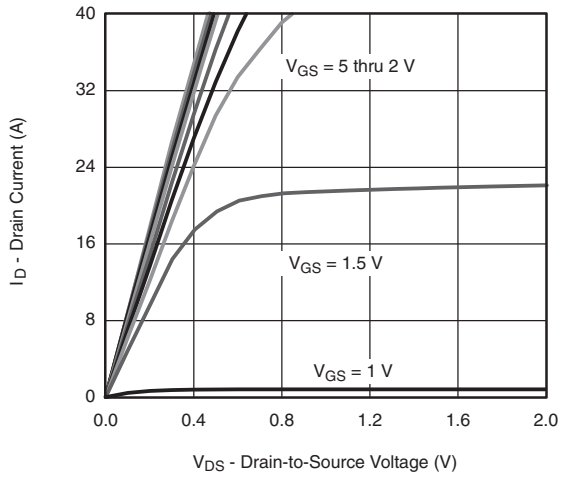
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		21		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 3.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250 µA	0.4		1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 7.7 A		0.012	0.015	Ω
		V_{GS} = 2.5 V, I_D = 7.3 A		0.014	0.017	
		V_{GS} = 1.8 V, I_D = 4.8 A		0.017	0.021	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 7.7 A		46		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		2100		pF
Output Capacitance	C_{oss}			310		
Reverse Transfer Capacitance	C_{rss}			180		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 8 V, I_D = 9.3 A		36	54	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 9.3 A		21	32	
Gate-Source Charge	Q_{gs}			3.3		
Gate-Drain Charge	Q_{gd}			3.1		
Gate Resistance	R_g	f = 1 MHz		5		Ω
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1.1 Ω $I_D \cong$ 9.3 A, V_{GEN} = 4.5 V, R_g = 1 Ω		10	15	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			15	25	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1.1 Ω $I_D \cong$ 9.3 A, V_{GEN} = 10 V, R_g = 1 Ω		7	15	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			55	85	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			12	A
Pulse Diode Forward Current	I_{SM}				40	
Body Diode Voltage	V_{SD}	I_S = 9.1 A, V_{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 9.3 A, dI/dt = 100 A/µs, T_J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			17	30	nC
Reverse Recovery Fall Time	t_a			12		ns
Reverse Recovery Rise Time	t_b			18		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing.

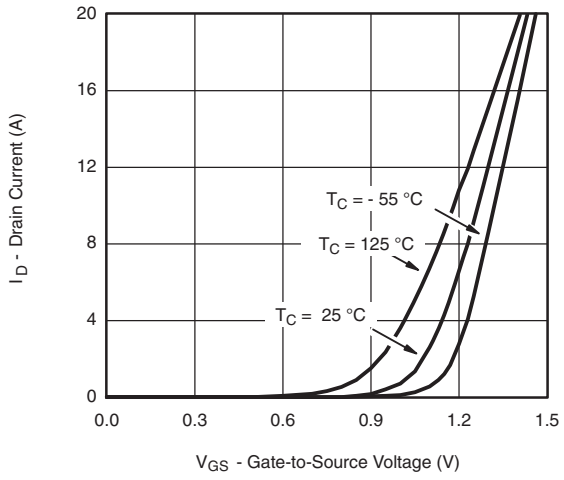
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 73783
S13-0194-Rev. C, 28-Jan-13

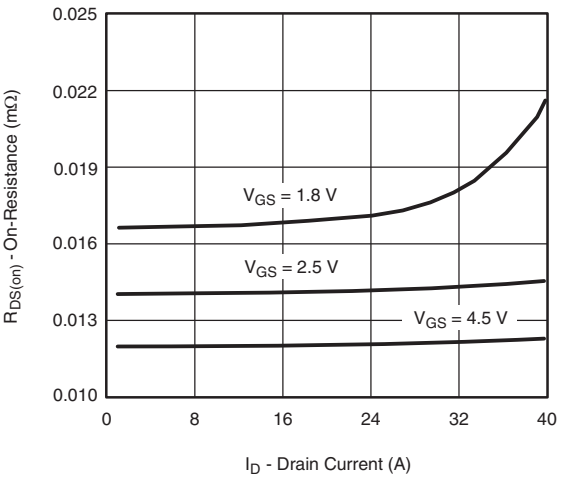
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



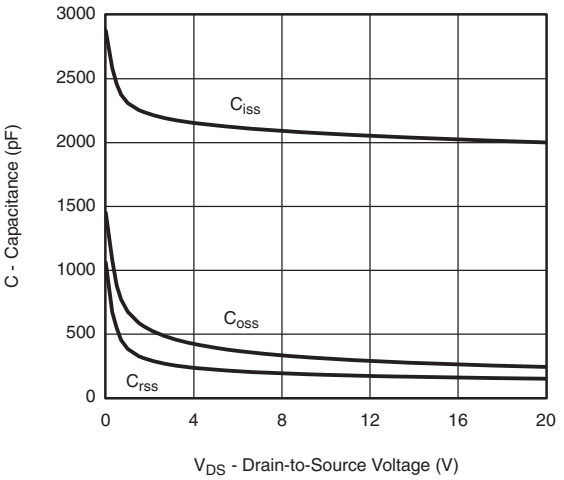
Output Characteristics



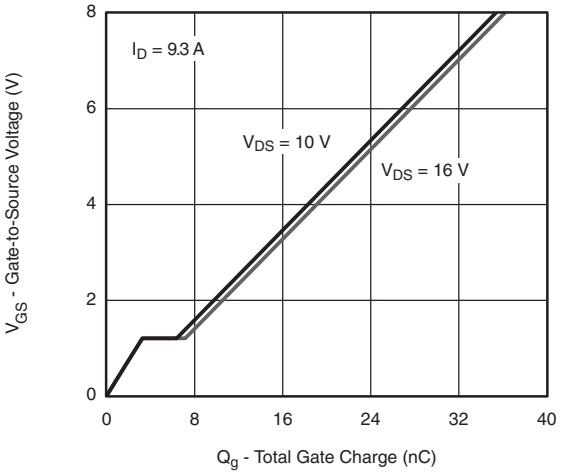
Transfer Characteristics



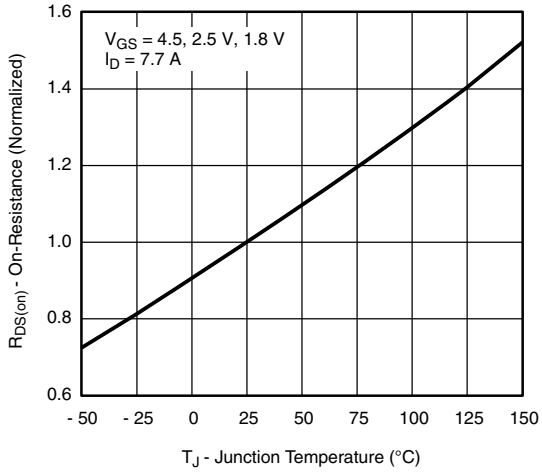
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

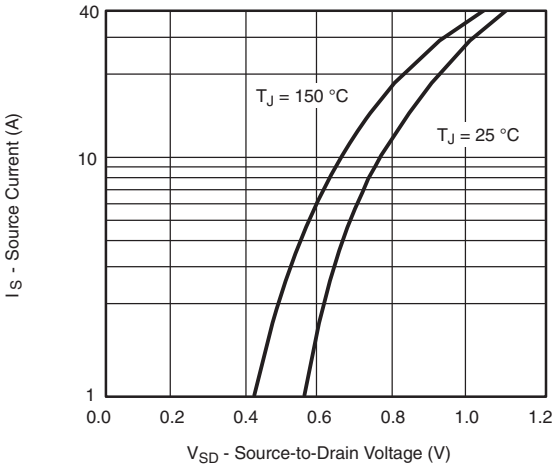


Gate Charge

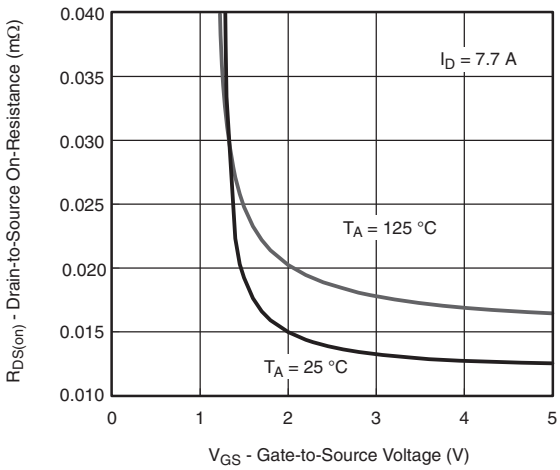


On-Resistance vs. Junction Temperature

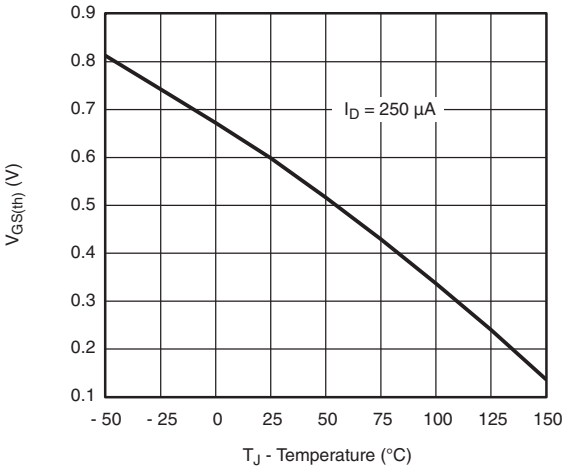
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



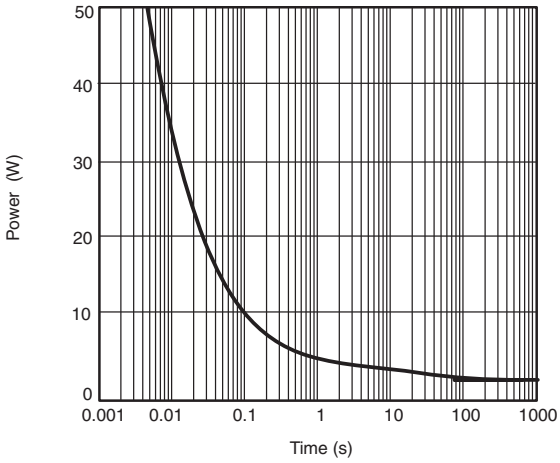
Source-Drain Diode Forward Voltage



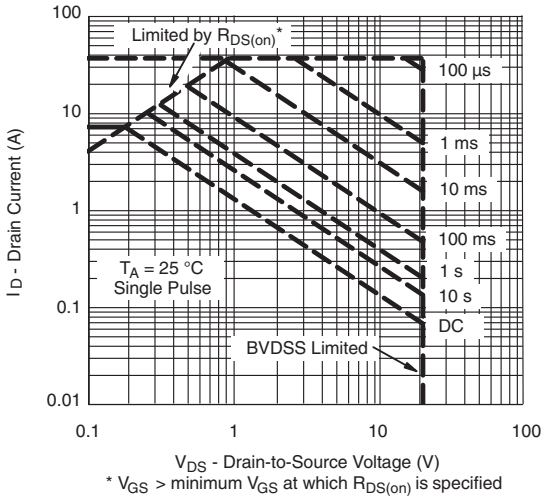
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

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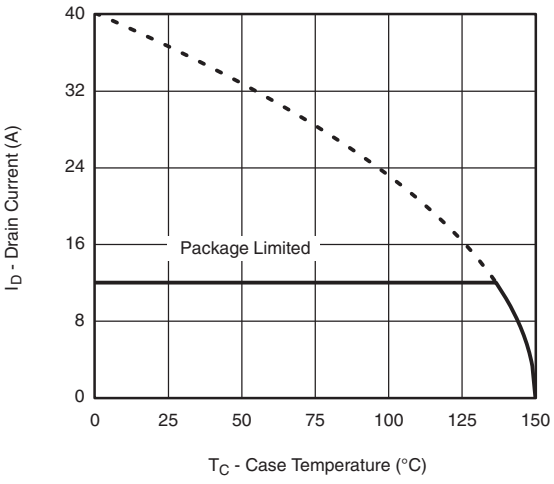
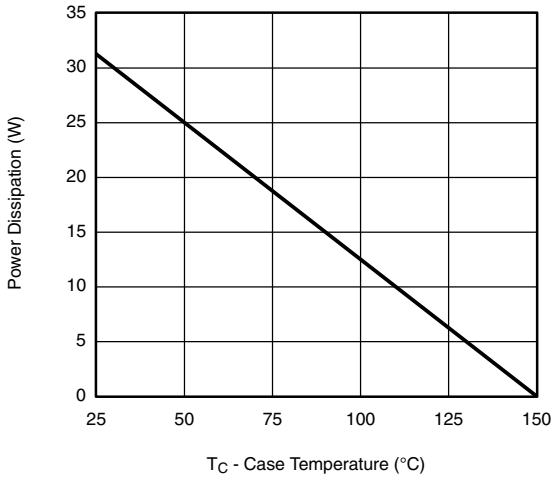


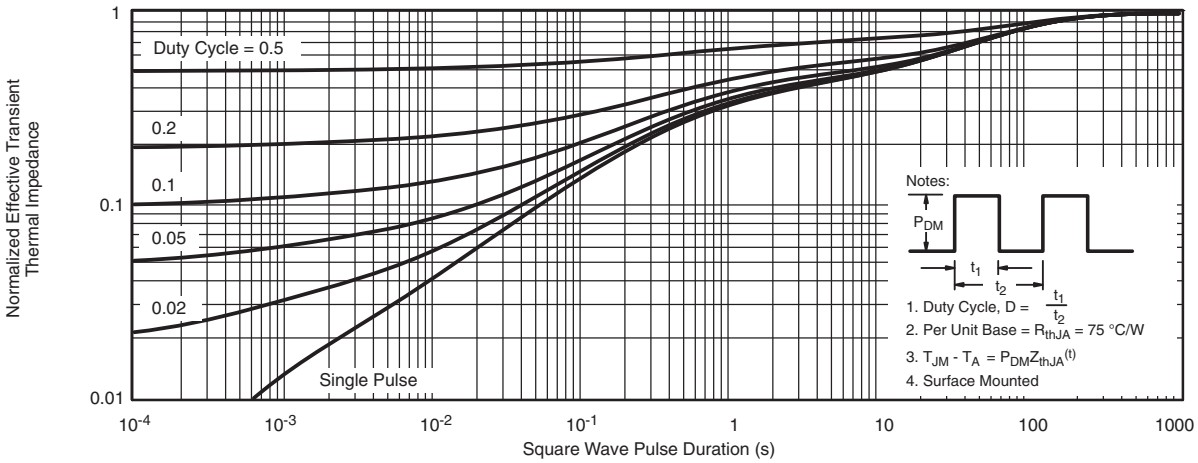
Current Derating*



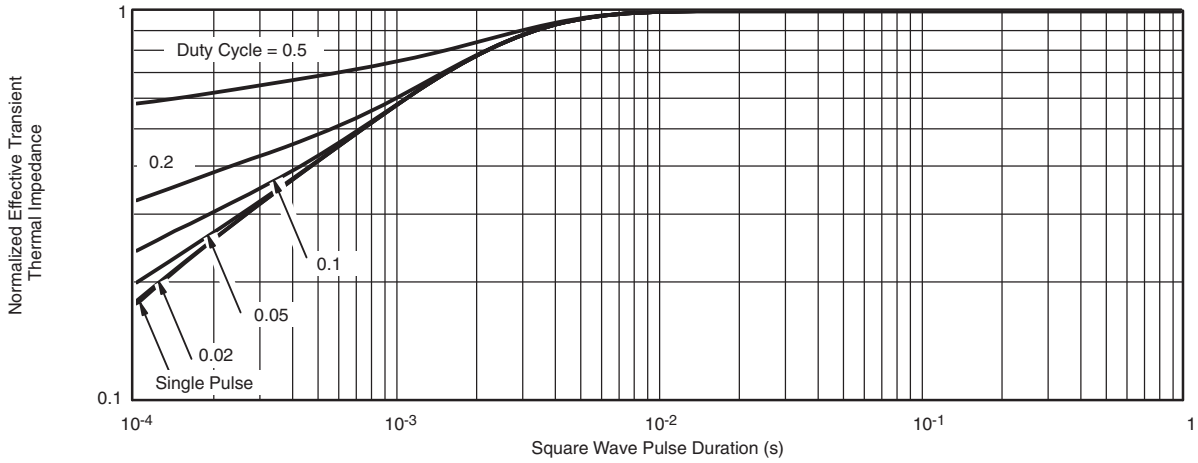
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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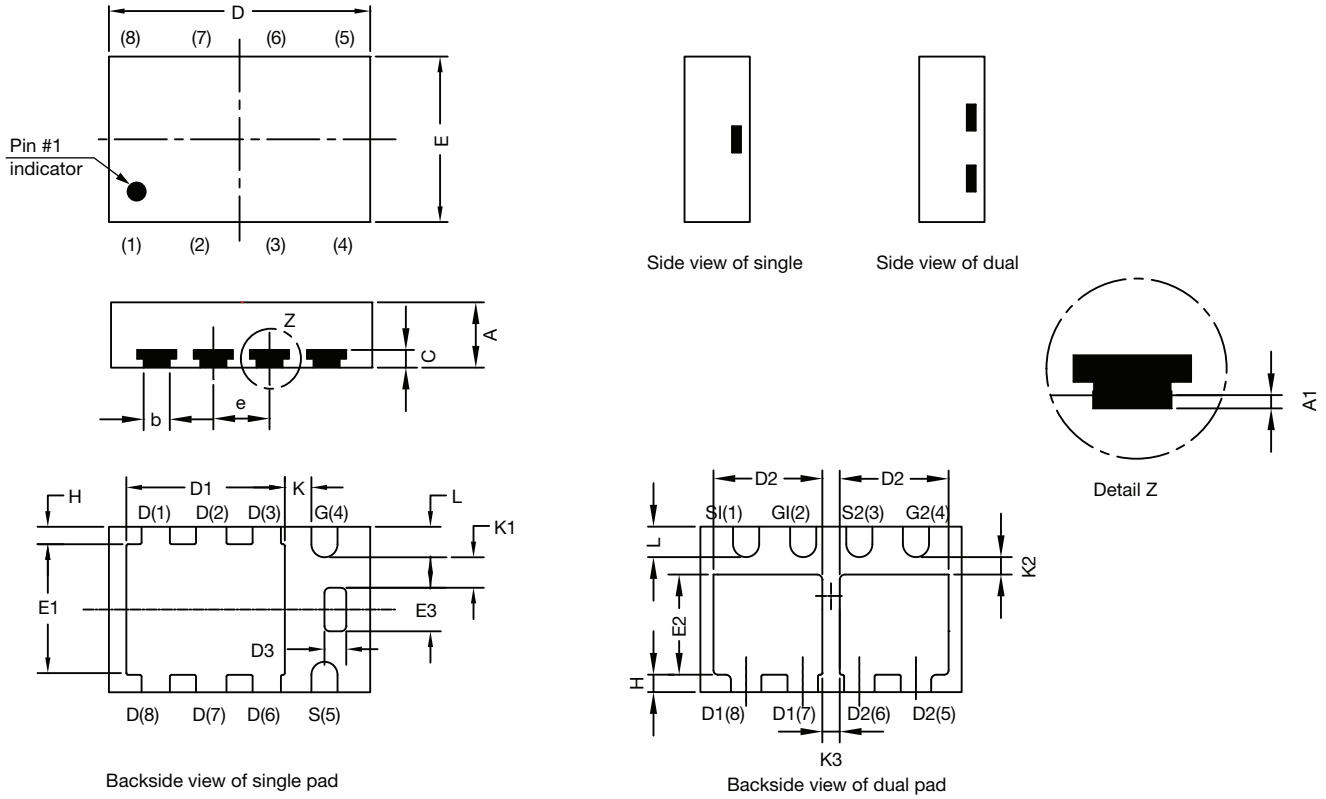
PowerPAK® ChipFET® Case Outline

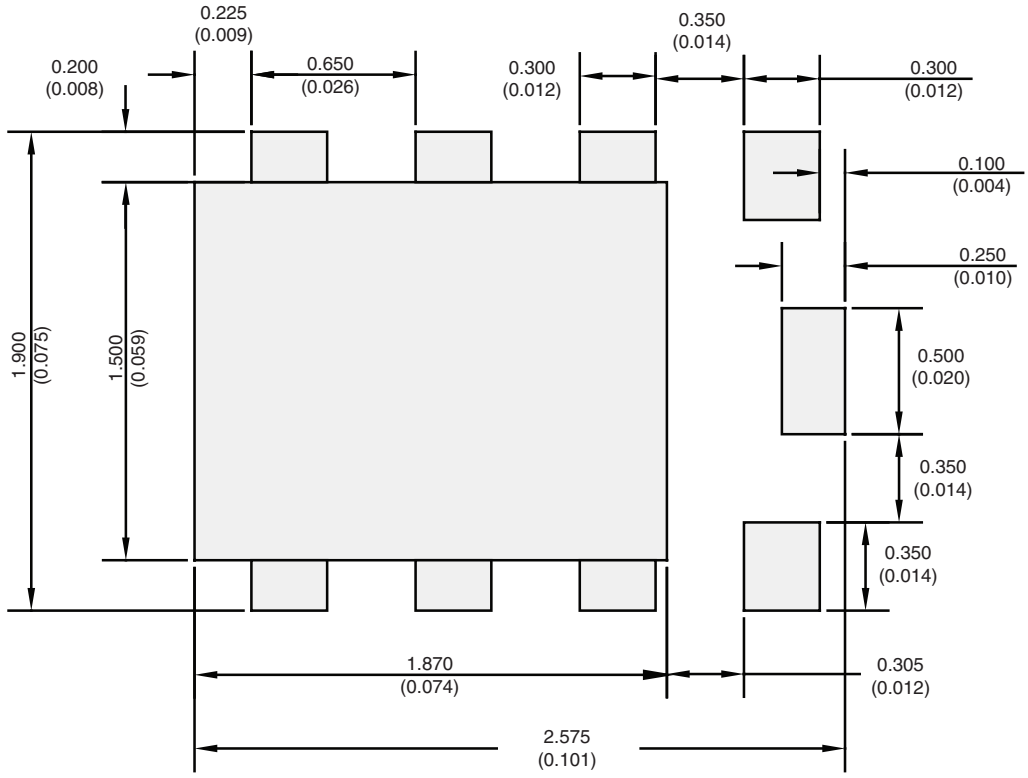


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14 DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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