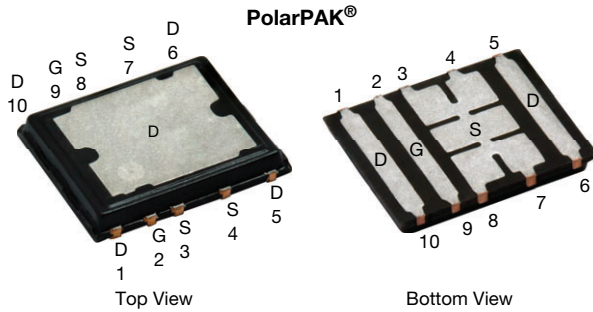


## N-Channel 20 V (D-S) MOSFET



Top surface is connected to pins 1, 5, 6, and 10

### FEATURES

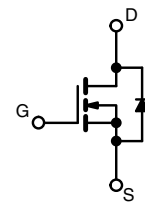
- TrenchFET® power MOSFET
- Ultra low thermal resistance using top-exposed PolarPAK® package for double-sided cooling
- Leadframe-based encapsulated package
  - Die not exposed
  - Same layout regardless of die size
- Low  $Q_{gd}/Q_{gs}$  ratio helps prevent shoot-through
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
**HALOGEN**  
**FREE**  
 Available

PRODUCT SUMMARY	
$V_{DS}$ (V)	20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0034
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0055
$Q_g$ typ. (nC)	24
$I_D$ (A) <sup>a</sup> (package limit)	50
$I_D$ (A) <sup>a</sup> (silicon limit)	138
Configuration	Single

### APPLICATIONS

- VRM
- DC/DC conversion
- Synchronous rectification



N-Channel MOSFET

ORDERING INFORMATION	
Package	PolarPAK
Lead (Pb)-free	SiE822DF-T1-E3
Lead (Pb)-free and halogen-free	SiE822DF-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	20	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	50 <sup>a</sup> (package limit)	A
		138 (silicon limit)	
		50 <sup>a</sup>	
		24.8 <sup>b, c</sup>	
Pulsed drain current	$I_{DM}$	80	A
Continuous source-drain diode current	$I_S$	50 <sup>a</sup>	
		4.3 <sup>b, c</sup>	
Single pulse avalanche current	$I_{AS}$	30	mJ
Avalanche energy	$E_{AS}$	45	
Maximum power dissipation	$P_D$	104	W
		66	
		5.2 <sup>b, c</sup>	
		3.3 <sup>b, c</sup>	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

### Notes

- Package limited is 50 A
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	20	24	°C/W
Maximum junction-to-case (drain top) <sup>a</sup>	Steady state	$R_{thJC}$ (drain)	1	1.2	
Maximum junction-to-case (source) <sup>a, c</sup>		$R_{thJC}$ (source)	2.8	3.4	

**Notes**

- a. Surface mounted on 1" x 1" FR4 board
- b. Maximum under steady state conditions is 68 °C/W
- c. Measured at source pin (on the side of the package)

SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	20	-	-	V	
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A	-	24.1	-	mV/°C	
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-7.1	-		
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	1.5	2.3	3.0	V	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V	-	-	$\pm 100$	nA	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 20$ V, $V_{GS} = 0$ V	-	-	1	$\mu$ A	
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	-	-	10		
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25	-	-	A	
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 18.3$ A	-	0.0028	0.0034	$\Omega$	
		$V_{GS} = 4.5$ V, $I_D = 14.5$ A	-	0.0045	0.0055		
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 18.3$ A	-	90	-	S	
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{ISS}$	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz	-	4200	-	pF	
Output capacitance	$C_{OSS}$		-	1000	-		
Reverse transfer capacitance	$C_{RSS}$		-	320	-		
Total gate charge	$Q_g$	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 20$ A	-	52	78	nC	
			$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A	-	24		36
				-	13		-
Gate-source charge	$Q_{gs}$	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A	-	5	-	nA	
Gate-drain charge	$Q_{gd}$		-	5	-		
Gate resistance	$R_g$		$f = 1$ MHz	-	1		1.5
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 1$ $\Omega$ , $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ $\Omega$	-	50	75	ns	
Rise time	$t_r$		-	220	330		
Turn-off delay time	$t_{d(off)}$		-	35	55		
Fall time	$t_f$		-	20	30		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20$ V, $R_L = 1$ $\Omega$ , $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$	-	15	25		
Rise time	$t_r$		-	25	40		
Turn-off delay time	$t_{d(off)}$		-	35	55		
Fall time	$t_f$		-	10	15		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	-	-	50	A	
Pulse diode forward current <sup>a</sup>	$I_{SM}$		-	-	80		
Body diode voltage	$V_{SD}$	$I_S = 10$ A	-	0.8	1.2	V	
Body diode reverse recovery time	$t_{rr}$	$I_F = 10$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C	-	40	60	ns	
Body diode reverse recovery charge	$Q_{rr}$		-	36	60	nC	
Reverse recovery fall time	$t_a$		-	19	-	ns	
Reverse recovery rise time	$t_b$		-	21	-		

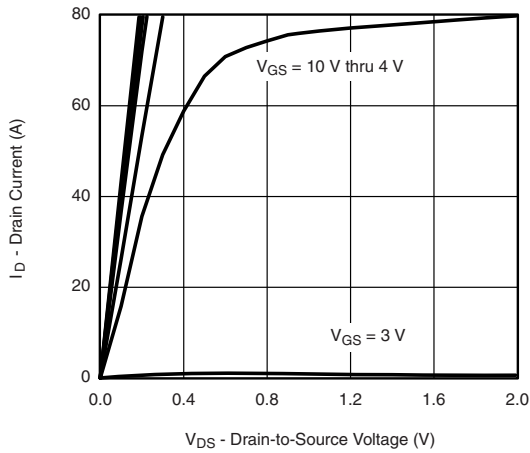
**Notes**

- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- b. Guaranteed by design, not subject to production testing

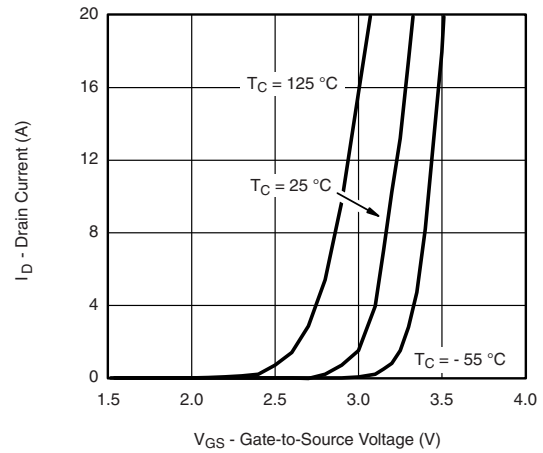
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



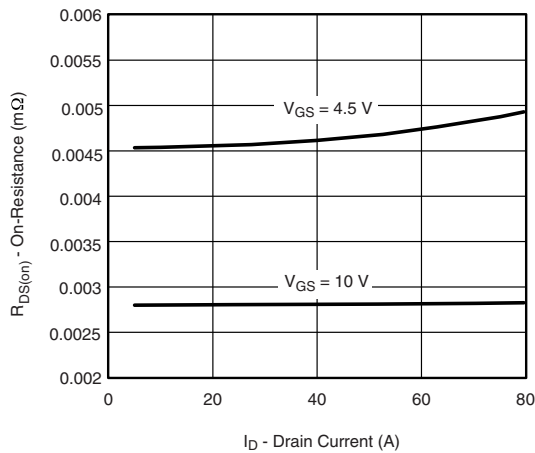
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



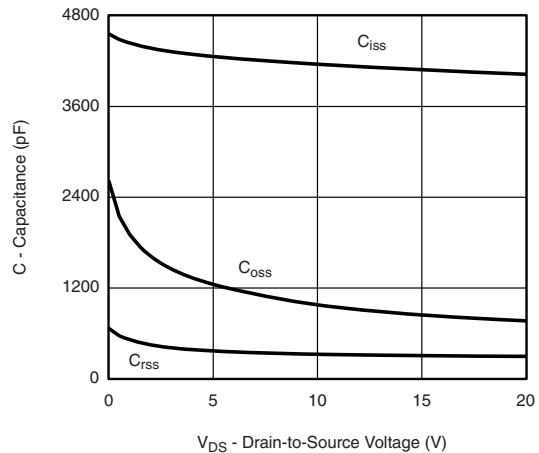
Output Characteristics



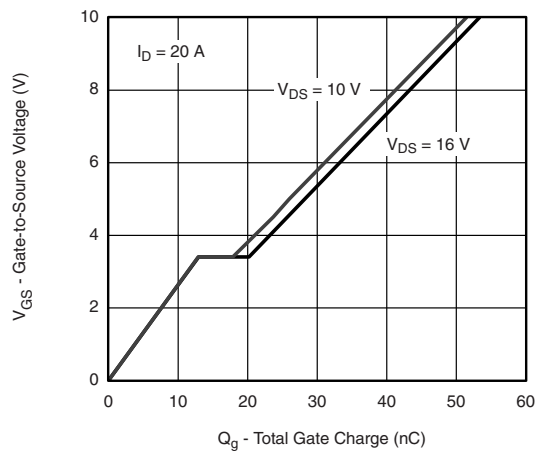
Transfer Characteristics



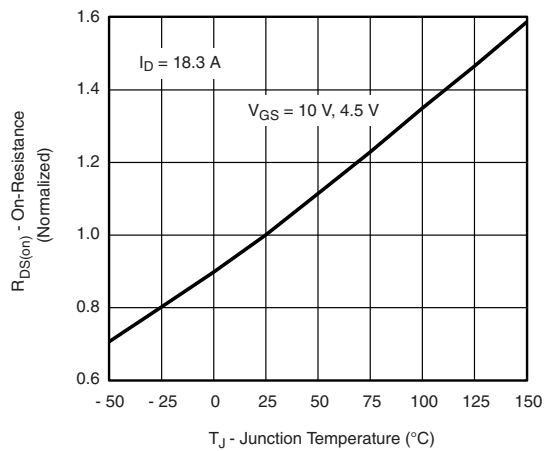
On-Resistance vs. Drain Current



Capacitance



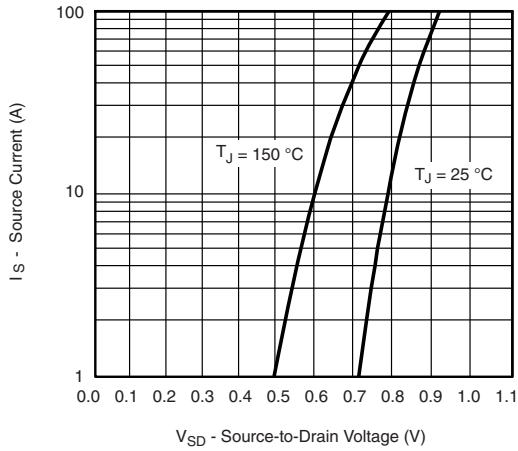
Gate Charge



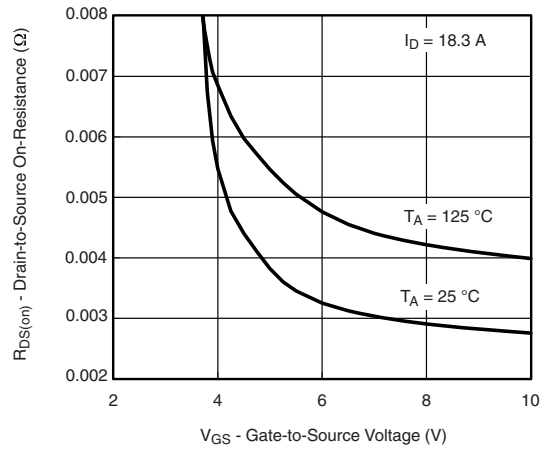
On-Resistance vs. Junction Temperature



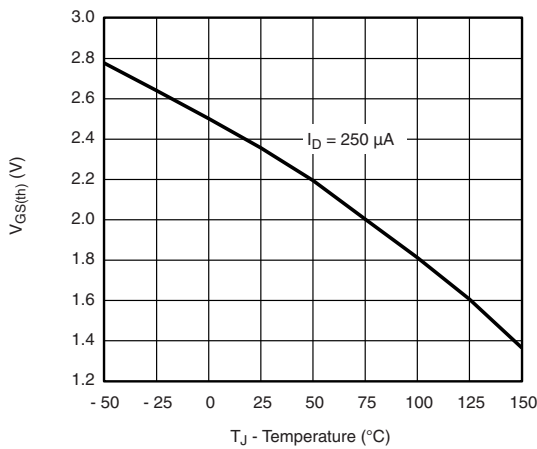
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



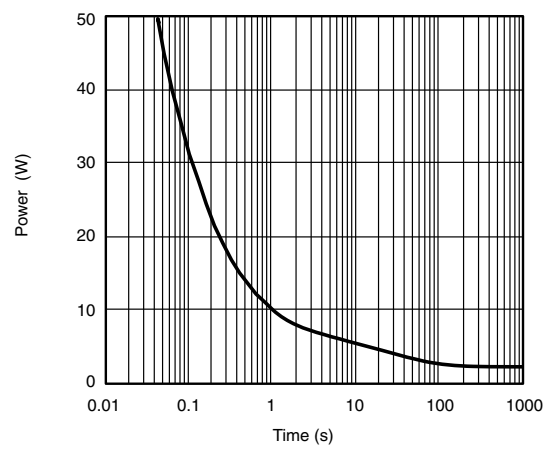
Source-Drain Diode Forward Voltage



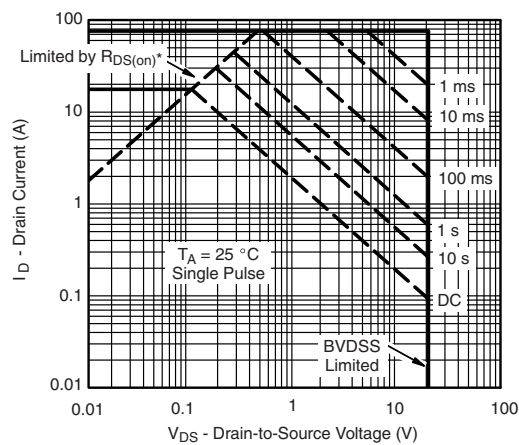
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



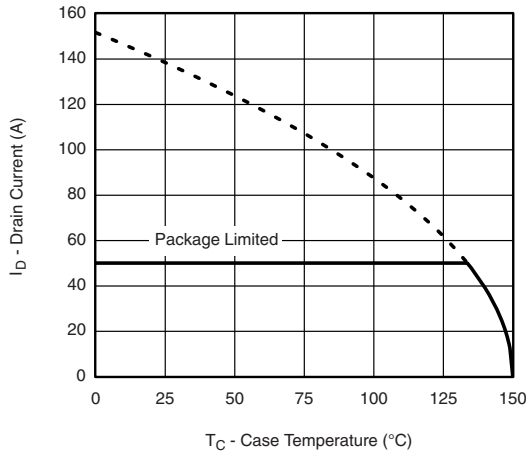
Single Pulse Power, Junction-to-Ambient



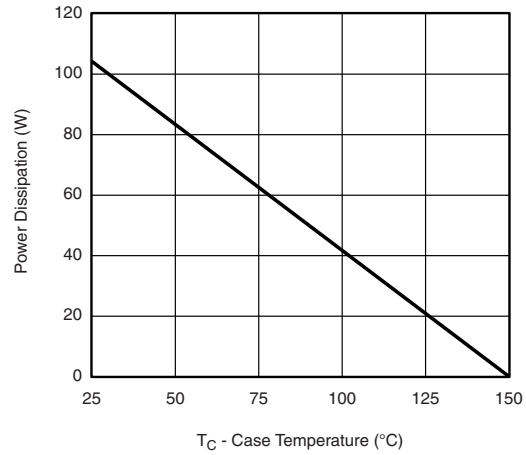
Safe Operating Area, Junction-to-Ambient



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**

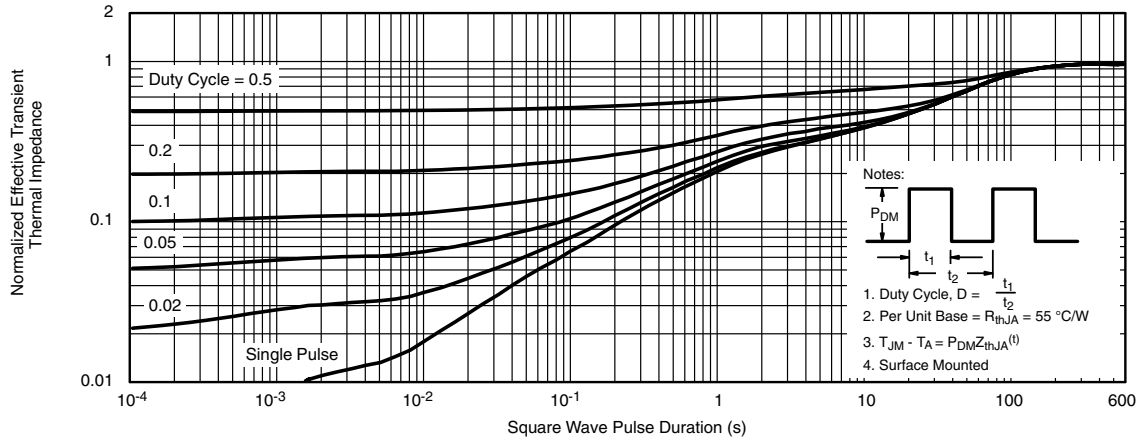


**Power Derating, Junction-to-Case**

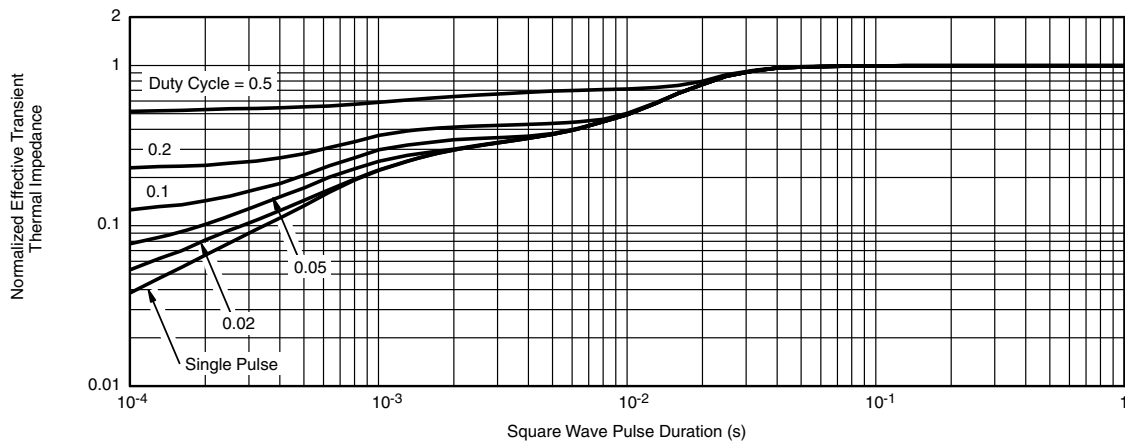
**Note**

- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

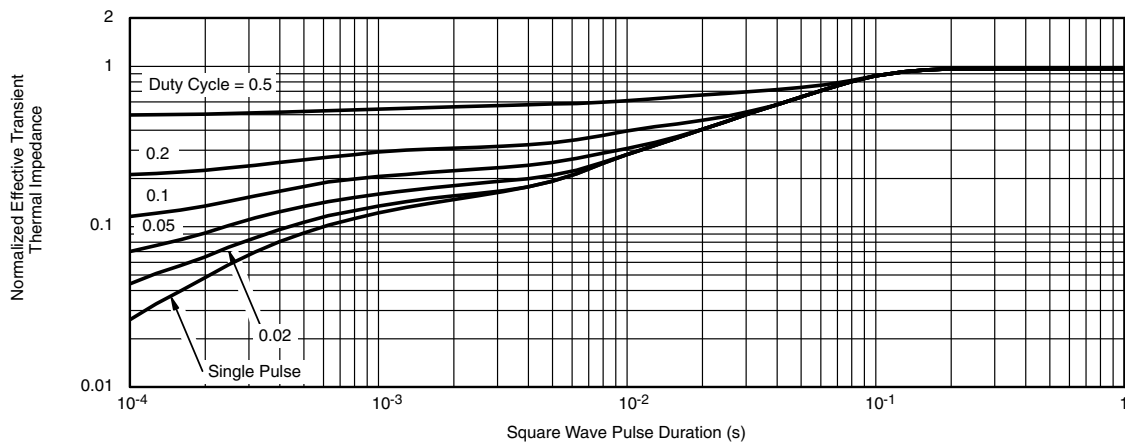
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)**



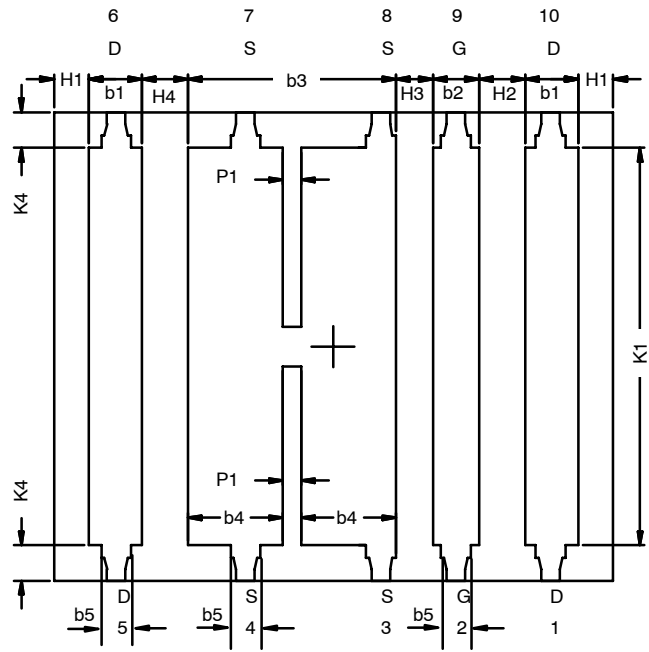
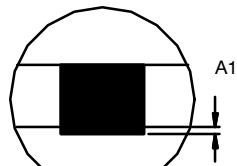
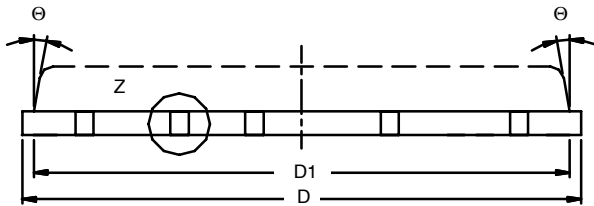
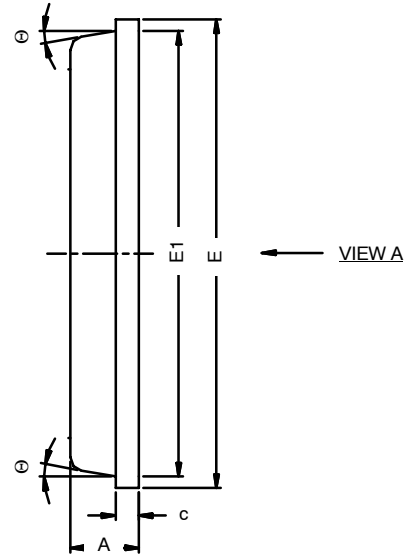
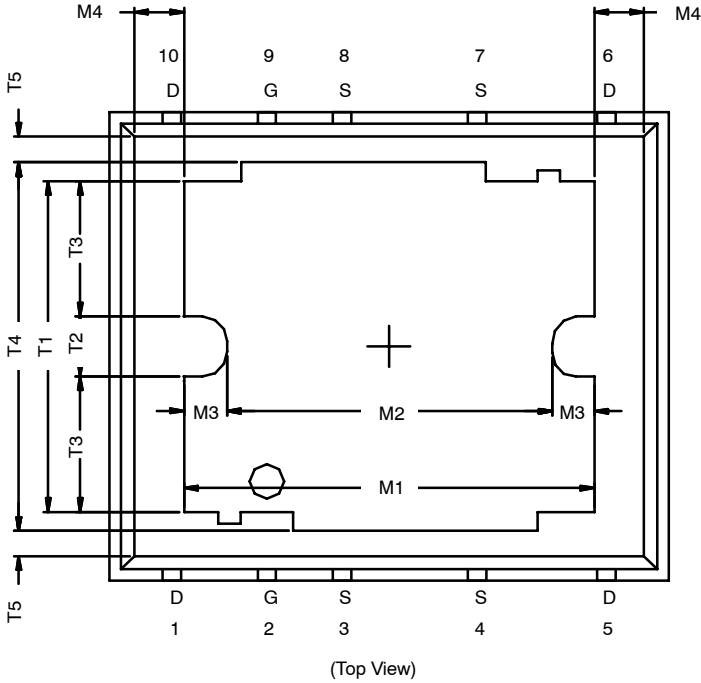
**Normalized Thermal Transient Impedance, Junction-to-Source**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?74451](http://www.vishay.com/ppg?74451).



**PolarPAK™ (Option S)**

Product datasheet/information page contain links to applicable package drawing.





Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	0.75	0.80	0.85	0.030	0.031	0.033
<b>A1</b>	0.00	–	0.05	0.000	–	0.002
<b>b1</b>	0.48	0.58	0.68	0.019	0.023	0.027
<b>b2</b>	0.41	0.51	0.61	0.016	0.020	0.024
<b>b3</b>	2.19	2.29	2.39	0.086	0.090	0.094
<b>b4</b>	0.89	1.04	1.19	0.035	0.041	0.047
<b>b5</b>	0.23	0.33	0.43	0.009	0.013	0.017
<b>c</b>	0.20	0.25	0.30	0.008	0.010	0.012
<b>D</b>	6.00	6.15	6.30	0.236	0.242	0.248
<b>D1</b>	5.74	5.89	6.04	0.226	0.232	0.238
<b>E</b>	5.01	5.16	5.31	0.197	0.203	0.209
<b>E1</b>	4.75	4.90	5.05	0.187	0.193	0.199
<b>H1</b>	0.23	–	–	0.009	–	–
<b>H2</b>	0.45	–	0.56	0.020	–	0.022
<b>H3</b>	0.31	0.41	0.51	0.012	0.016	0.020
<b>H4</b>	0.45	–	0.56	0.020	–	0.022
<b>K1</b>	4.22	4.37	4.52	0.166	0.172	0.178
<b>K4</b>	0.24	–	–	0.009	–	–
<b>M1</b>	4.30	4.50	4.70	0.169	0.177	0.185
<b>M2</b>	3.43	3.58	3.73	0.135	0.141	0.147
<b>M3</b>	0.22	–	–	0.009	–	–
<b>M4</b>	0.05	–	–	0.002	–	–
<b>P1</b>	0.15	0.20	0.25	0.006	0.008	0.010
<b>T1</b>	3.48	3.64	4.10	0.137	0.143	0.150
<b>T2</b>	0.56	0.76	0.95	0.22	0.030	0.037
<b>T3</b>	1.20	–	–	0.051	–	–
<b>T4</b>	3.90	–	–	0.154	–	–
<b>T5</b>	0	0.18	0.36	0.000	0.007	0.014
<b>Θ</b>	0°	10°	12°	0°	10°	12°
ECN: S-51049—Rev. B, 13-Jun-05 DWG: 5947						

Note: Millimeters govern over inches



## RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S  
 Dimensions in mm/(Inches)  
 No External Traces within Broken Lines  
 Dot indicates Gate Pin (Part Marking)



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