

Automotive N- and P-Channel 100 V (D-S) 175 °C MOSFET

DESCRIPTION

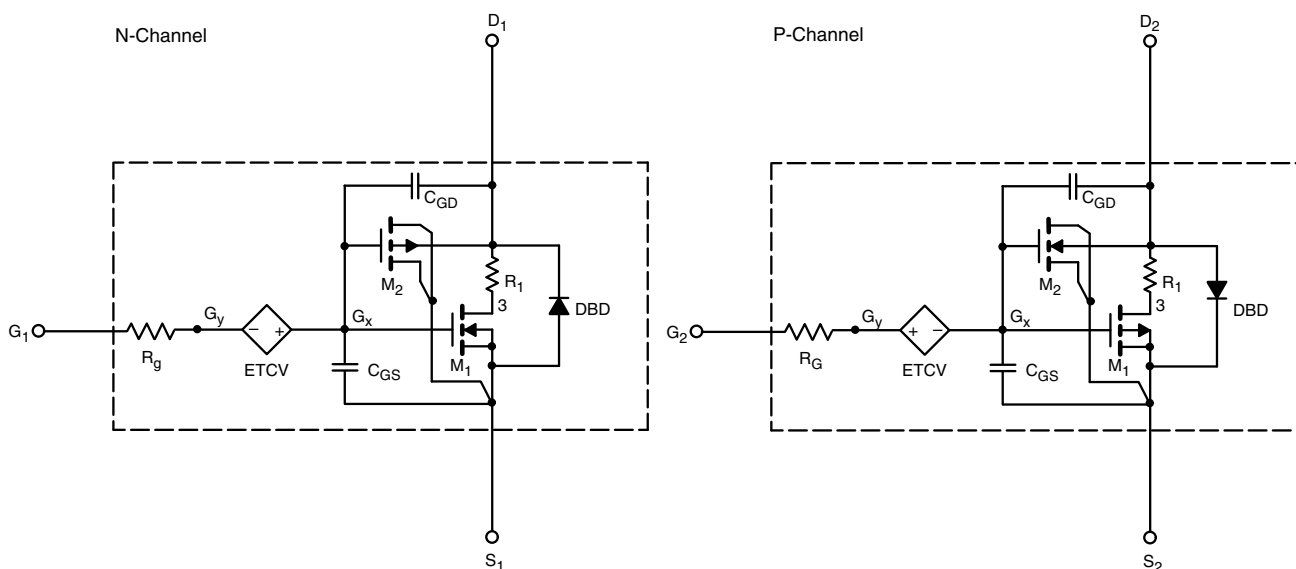
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	2	2	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	2	2	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 6 A	N-Ch	0.0351	0.0365	Ω
		V _{GS} = -10 V, I _D = -6 A	P-Ch	0.1233	0.1184	
		V _{GS} = 4.5 V, I _D = 4 A	N-Ch	0.0510	0.0468	
		V _{GS} = -4.5 V, I _D = -4 A	P-Ch	0.1800	0.1669	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 6 A	N-Ch	13	15	S
		V _{DS} = -15 V, I _D = -6 A	P-Ch	7.2	7	
Diode Forward Voltage ^a	V _{SD}	I _S = 6 A	N-Ch	0.86	0.89	V
		I _S = -6 A	P-Ch	-0.86	-0.89	
Dynamic ^b						
Input Capacitance	C _{iss}	N-Channel V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -25 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	450	420	pF
Output Capacitance	C _{oss}		P-Ch	588	480	
			N-Ch	260	260	
Reverse Transfer Capacitance	C _{rss}		P-Ch	240	250	
			N-Ch	16	17	
Total Gate Charge	Q _g		P-Ch	29	20	
		N-Channel V _{DS} = 50 V, V _{GS} = 10 V, I _D = 1 A P-Channel V _{DS} = -50 V, V _{GS} = -10 V, I _D = -1 A	N-Ch	8	9	nC
Gate-Source Charge	Q _{gs}		P-Ch	10.2	12	
			N-Ch	1.2	1.2	
Gate-Drain Charge	Q _{gd}		P-Ch	1.7	2	
			N-Ch	1.8	1.9	
	P-Ch		3.3	3		

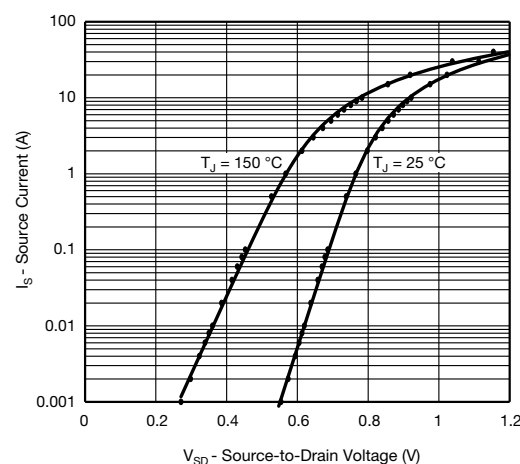
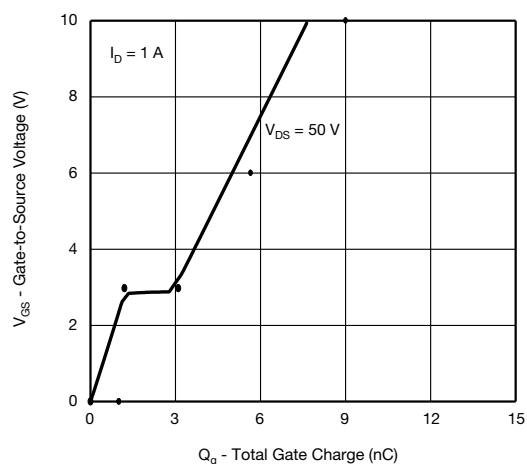
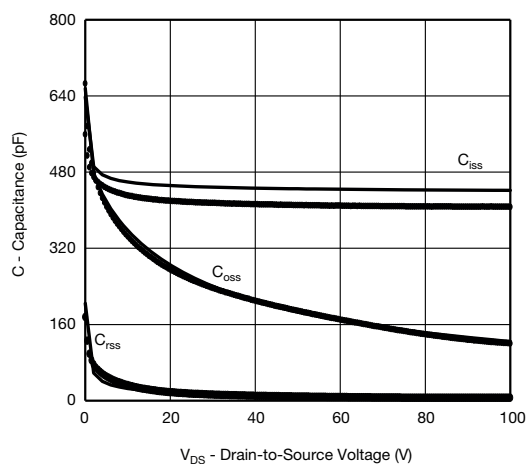
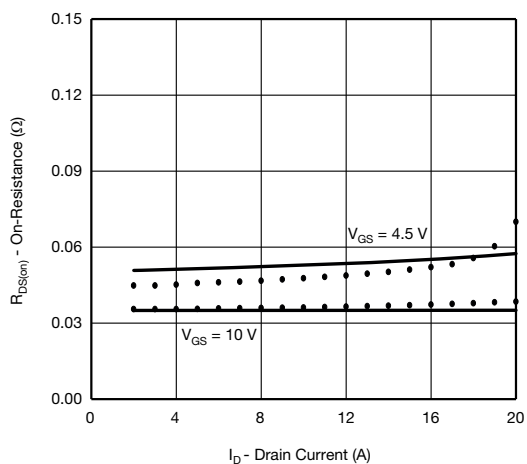
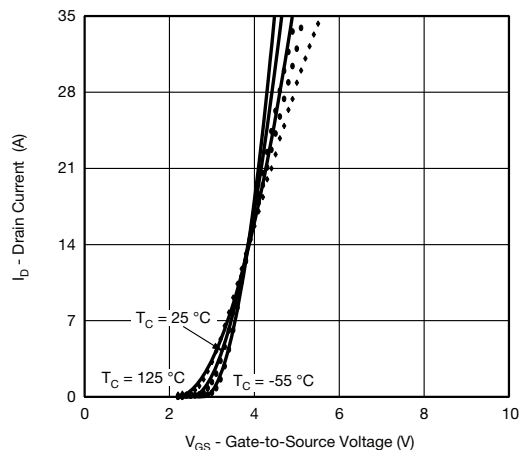
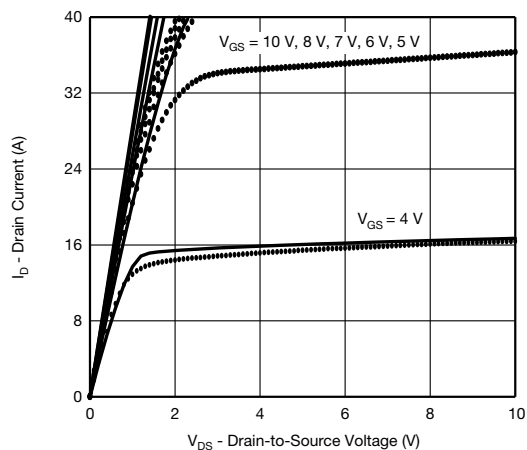
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$, unless otherwise noted

N-Channel MOSFET



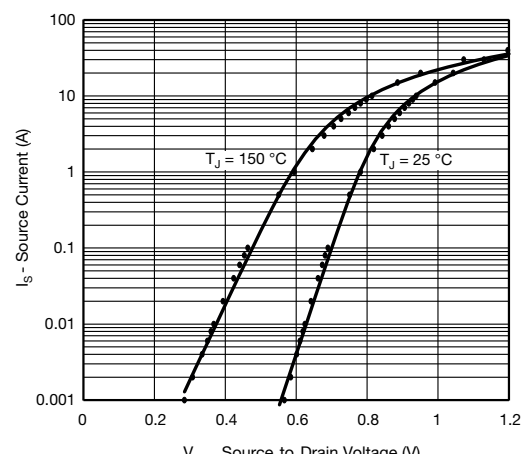
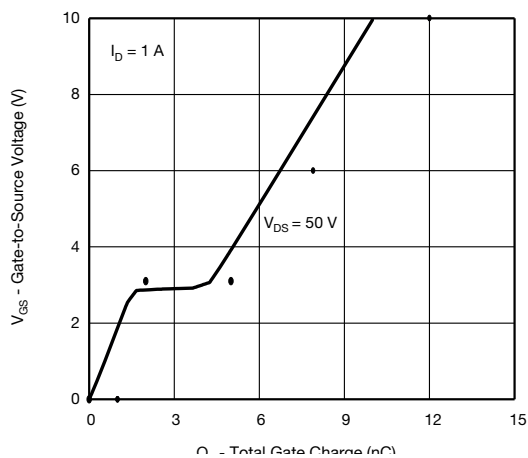
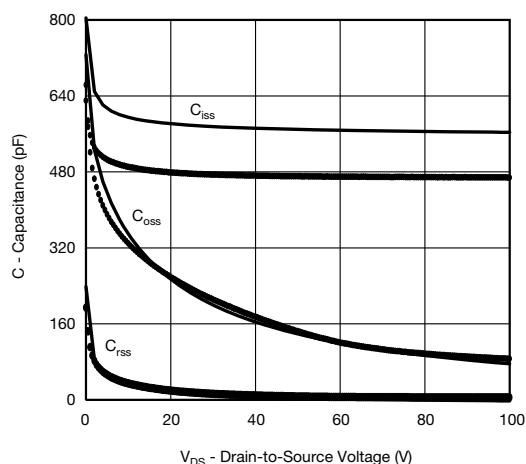
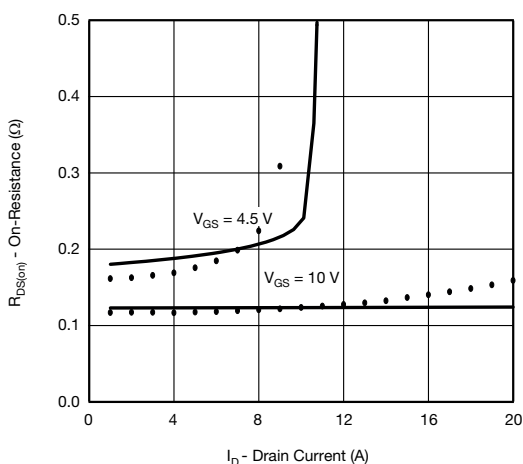
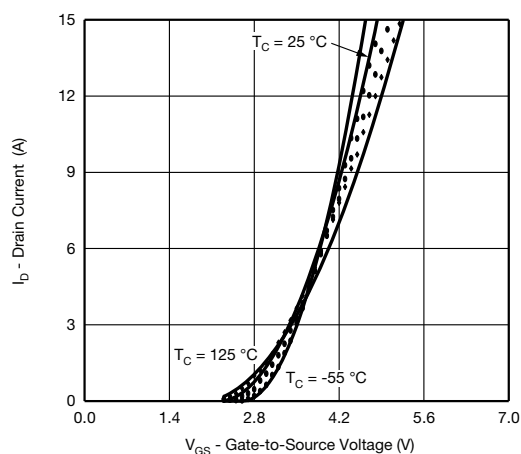
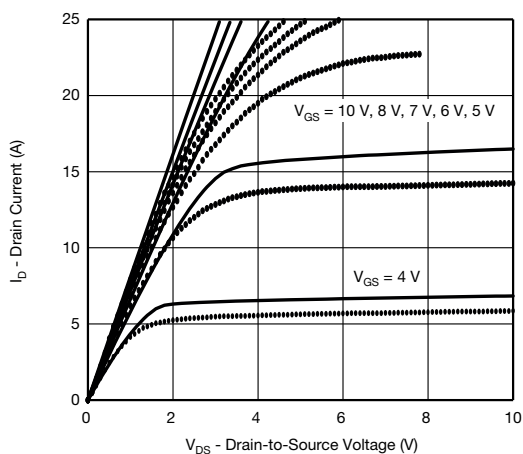
Note

- Dots and squares represent measured data.



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P-Channel MOSFET



Note

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