Vishay Siliconix

# N-Channel 100 V (D-S) MOSFET

## **DESCRIPTION**

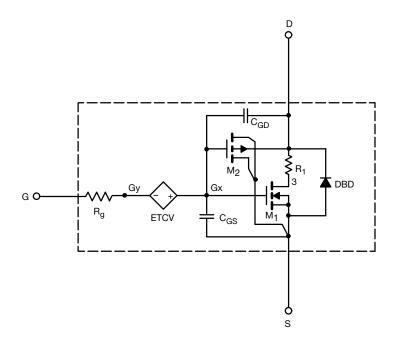
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- · Model the gate charge

## SUBCIRCUIT MODEL SCHEMATIC



## Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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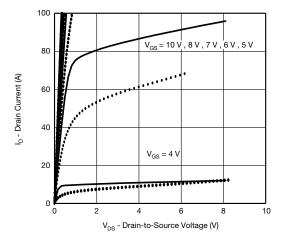
<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	0.043	0.045	Ω
		$V_{GS} = 7.5 \text{ V}, I_D = 4 \text{ A}$	0.046	0.051	
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	17	25	S
Diode forward voltage	$V_{SD}$	I <sub>S</sub> = 4 A	0.82	0.85	V
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	595	550	pF
Output capacitance	Coss		52	50	
Reverse transfer capacitance	C <sub>rss</sub>		7.4	7	
Total gate charge	$Q_g$	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	8.1	8.5	- nC
		$V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 4 \text{ A}$	6.1	6.5	
Gate-source charge	$Q_{gs}$		2.5	2.5	
Gate-drain charge	$Q_{gd}$		1.5	1.5	

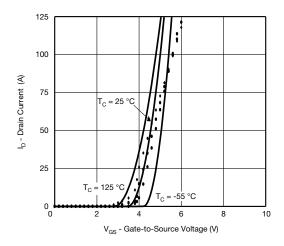
#### Notes

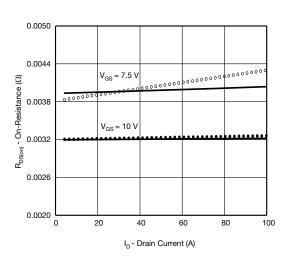
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

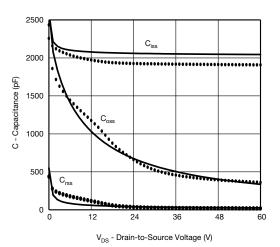
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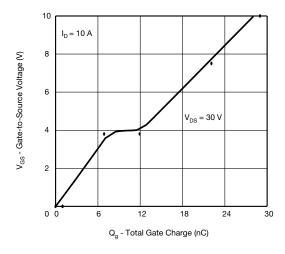
## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25$ °C, unless otherwise noted)

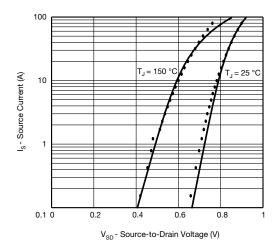












## Note

 Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.



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