

P-Channel 30 V (D-S) MOSFET

DESCRIPTION

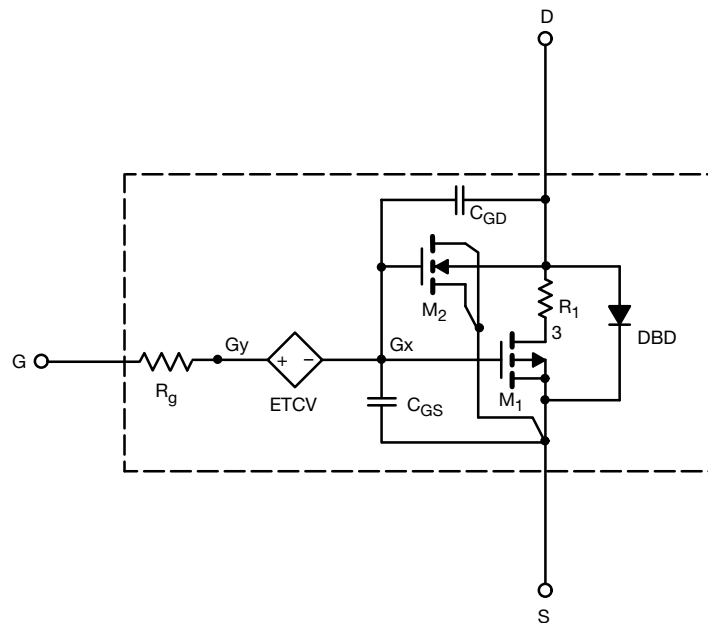
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



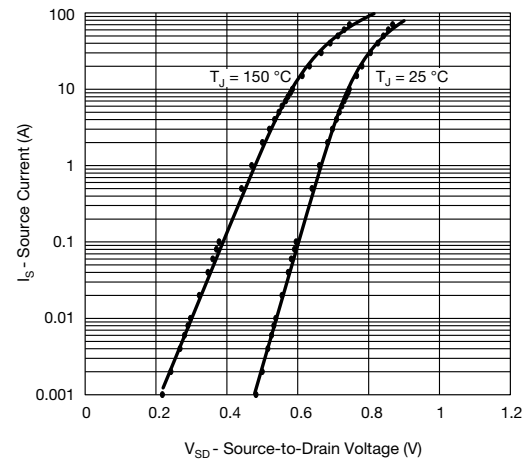
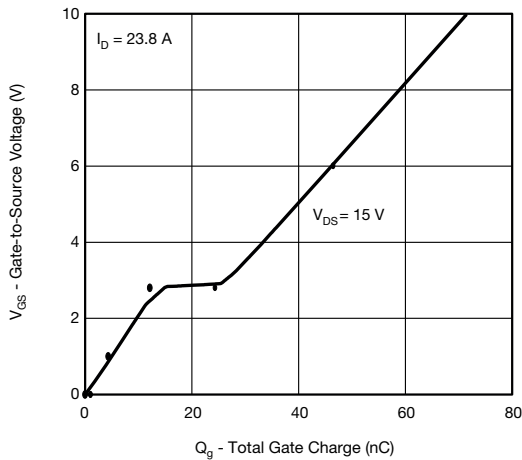
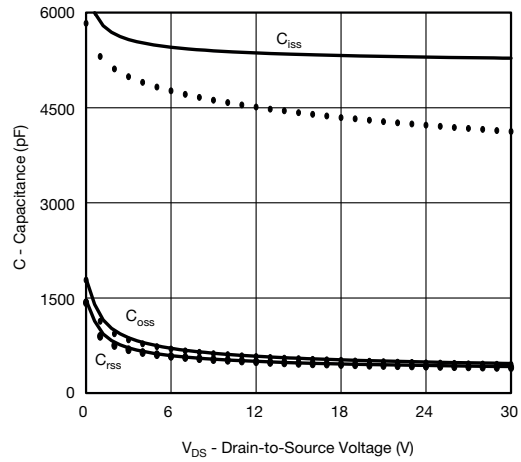
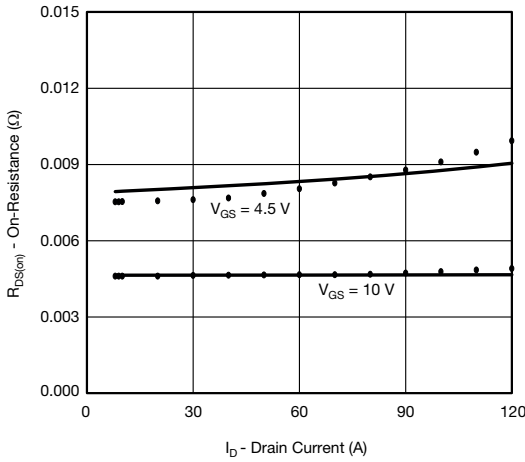
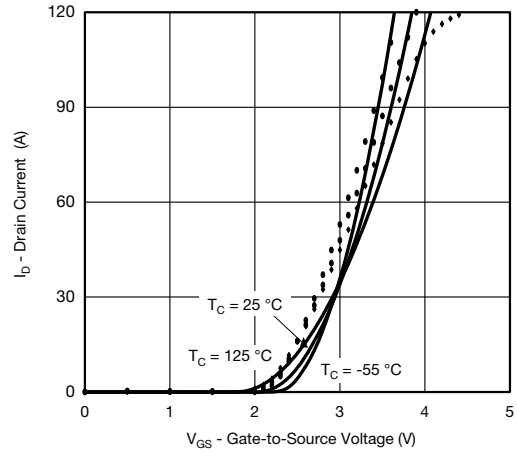
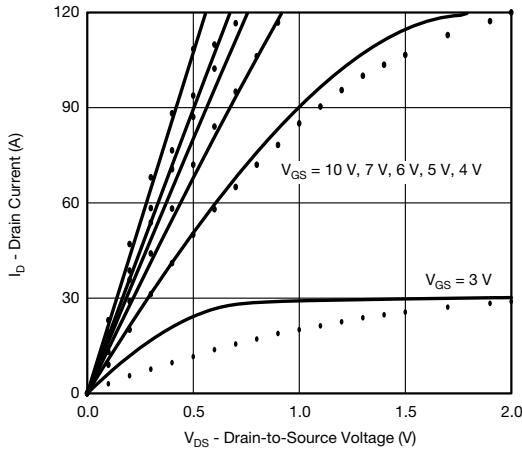
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	1.8	-	V
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -15\text{ A}$	0.0046	0.0046	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$	0.0079	0.0078	
Forward transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -20\text{ A}$	48	60	S
Diode forward voltage	V_{SD}	$I_S = -5\text{ A}$	-0.73	-0.73	V
Dynamic ^b					
Input capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	5340	4380	pF
Output capacitance	C_{oss}		548	535	
Reverse transfer capacitance	C_{rss}		471	460	
Total gate charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -23.8\text{ A}$	72	74	nC
Gate-source charge	Q_{gs}	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -23.8\text{ A}$	37	36	
Gate-drain charge	Q_{gd}		12	12.1	
			12	12.3	

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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