

N- and P-Channel 20 V (D-S) MOSFET

DESCRIPTION

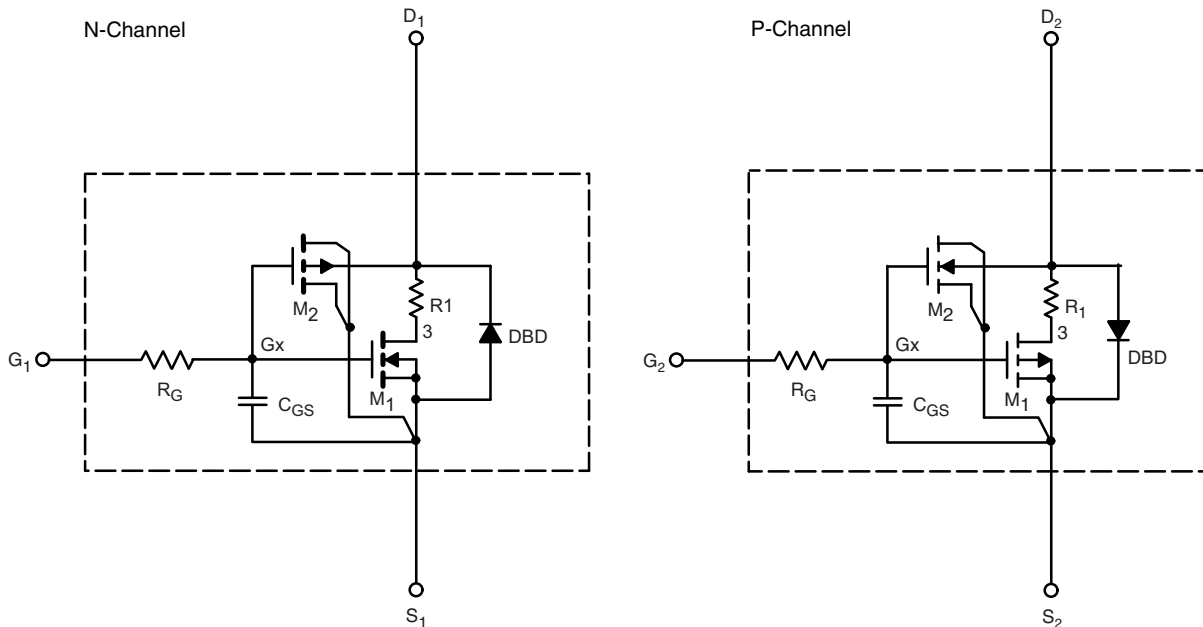
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and p-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to 125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



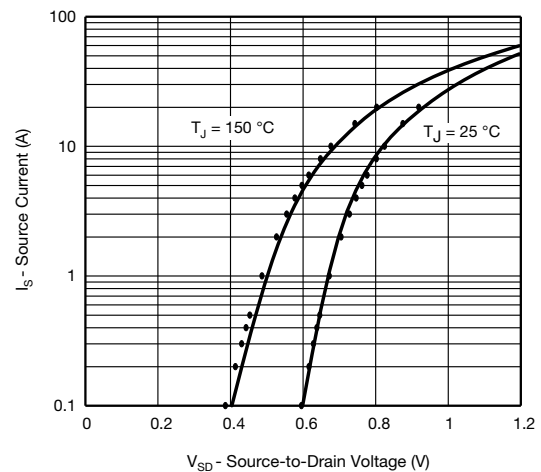
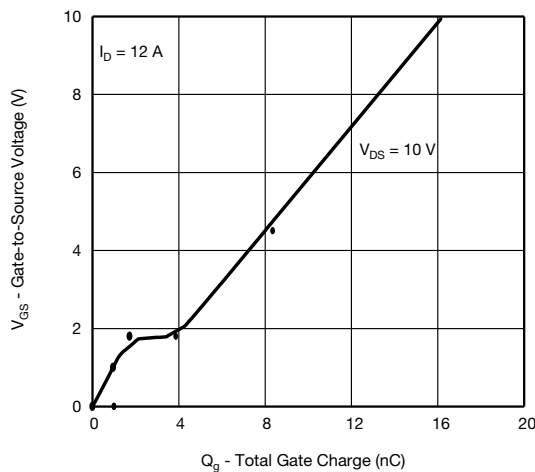
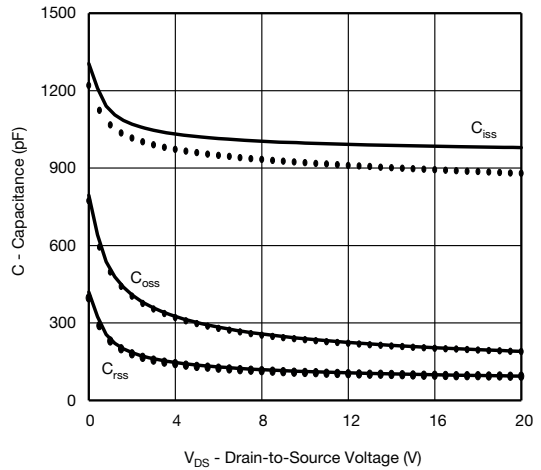
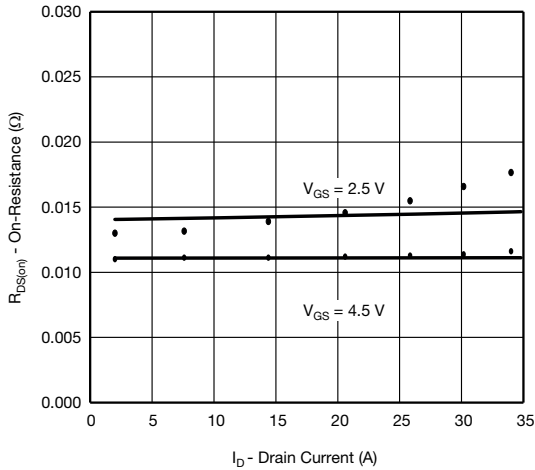
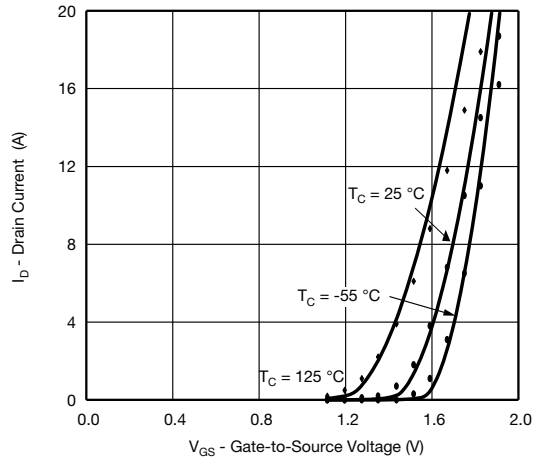
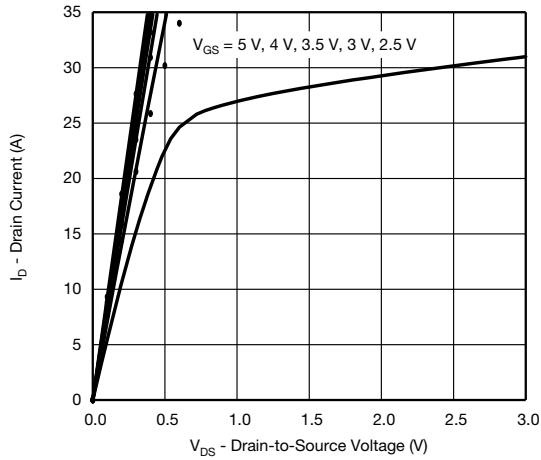
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT	
Static							
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.1	-	V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	1.1	-		
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 12 A	N-Ch	0.0111	0.0115	Ω	
		V _{GS} = -4.5 V, I _D = -9 A	P-Ch	0.0235	0.0220		
		V _{GS} = 2.5 V, I _D = 9 A	N-Ch	0.0143	0.0150		
		V _{GS} = -2.5 V, I _D = -6 A	P-Ch	0.0360	0.0330		
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 12 A	N-Ch	72	55	S	
		V _{DS} = -10 V, I _D = -9 A	P-Ch	26	24		
Diode forward voltage ^a	V _{SD}	I _S = 2.9 A	N-Ch	0.74	0.80	V	
		I _S = -2.9 A	P-Ch	-0.76	-0.81		
Dynamic ^b							
Input capacitance	C _{iss}	N-channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	997	915	pF	
Output capacitance	C _{oss}		P-Ch	1500	1310		
Reverse transfer capacitance	C _{rss}	P-channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	239	235		
			P-Ch	298	310		
Total gate charge	Q _g	N-channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 12 A	N-Ch	17	18		nC
			P-Ch	30	32		
Gate-source charge	Q _{gs}	P-channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -9 A	N-Ch	8.1	8.5		
			P-Ch	15	16		
Gate-drain charge	Q _{gd}		N-Ch	1.8	1.8		
			P-Ch	2.2	2.3		

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing



N-CHANNEL COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)

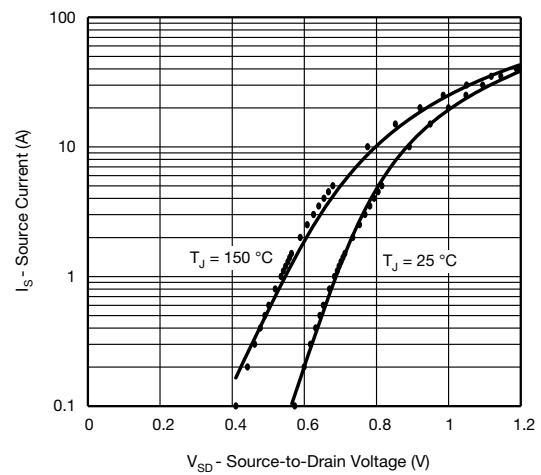
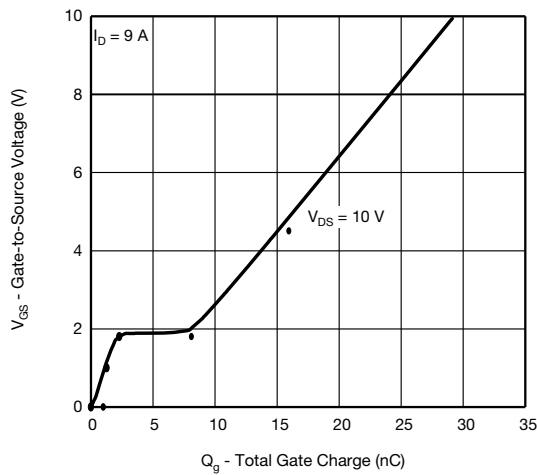
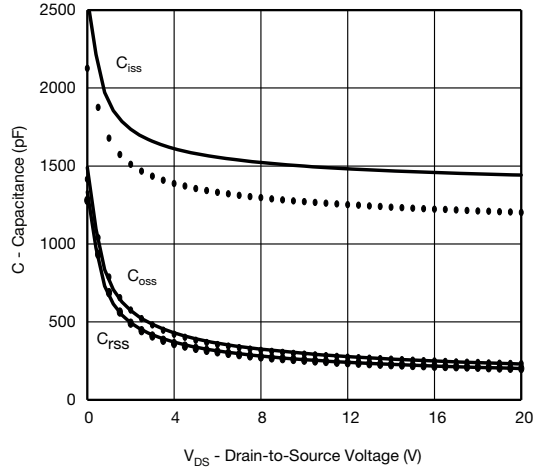
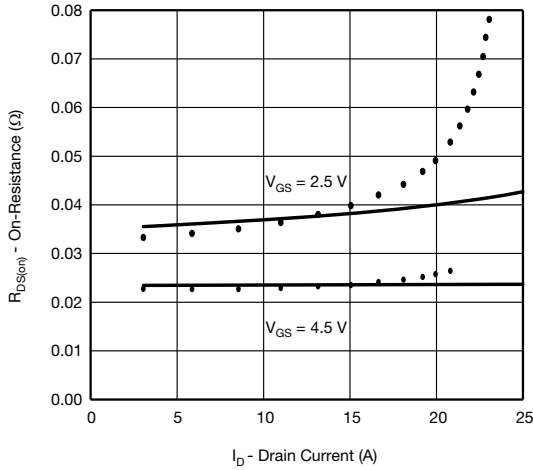
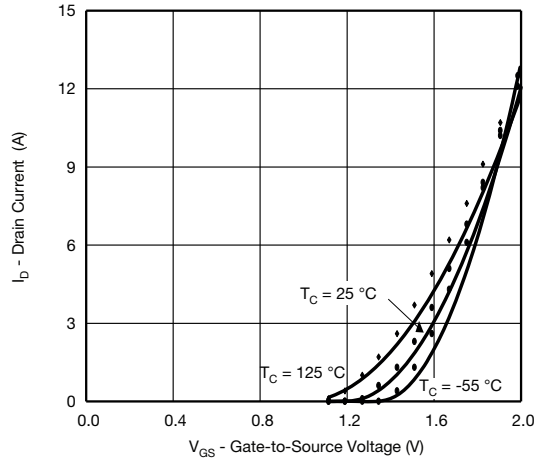
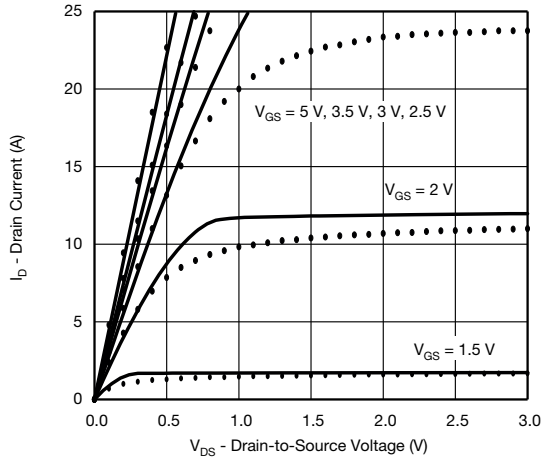


Note

- Dots and squares represent measured data



P-CHANNEL COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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