

## N-Channel 100 V (D-S) 200 ° MOSFET

### DESCRIPTION

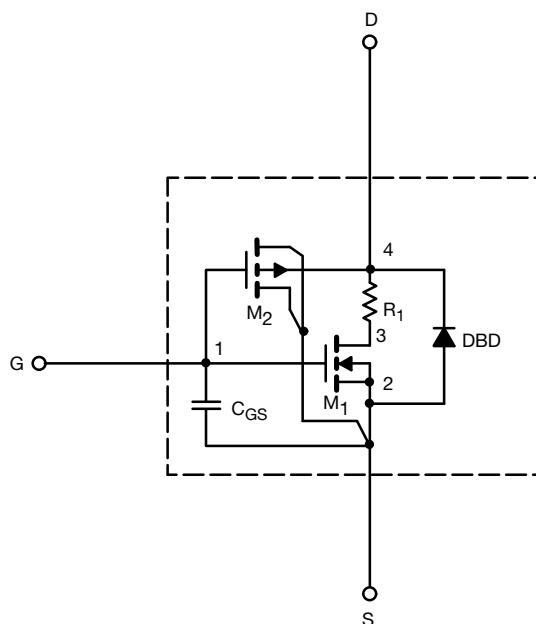
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



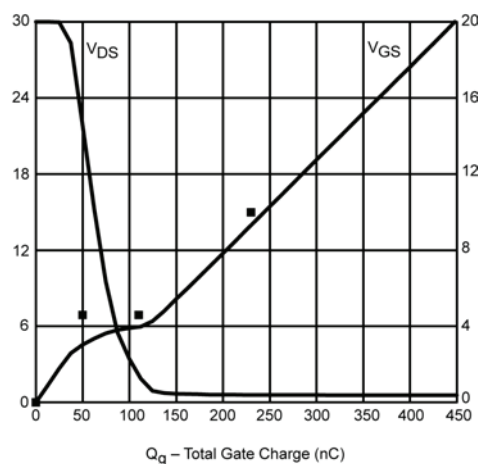
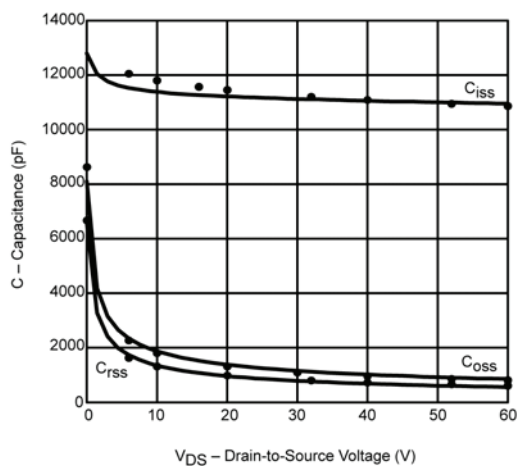
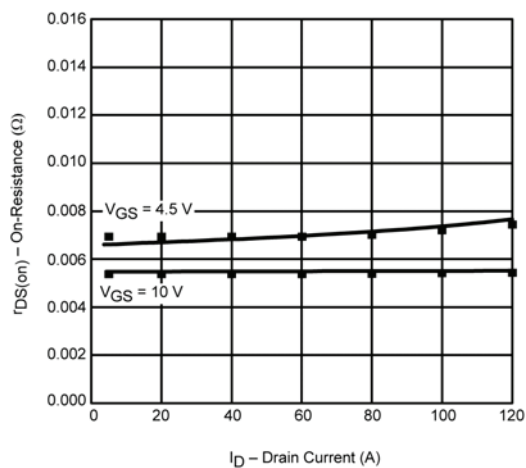
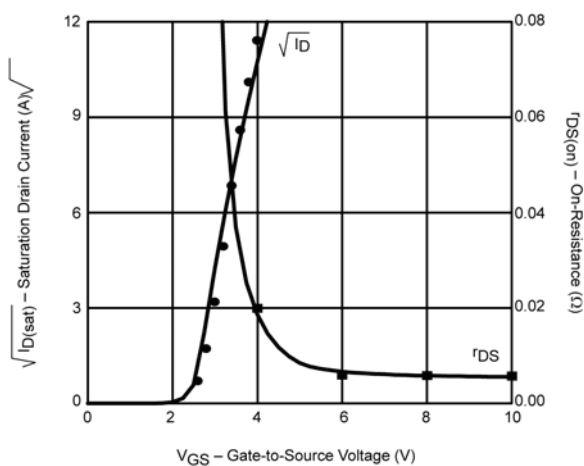
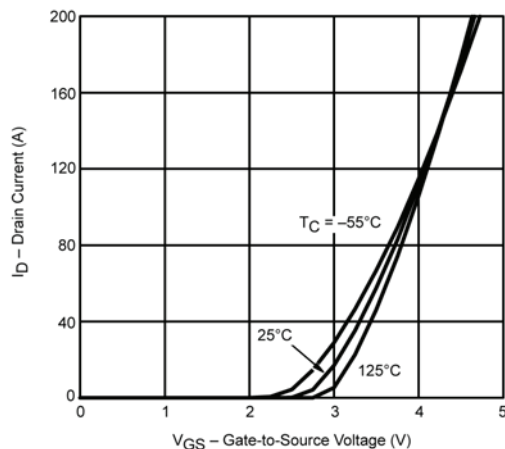
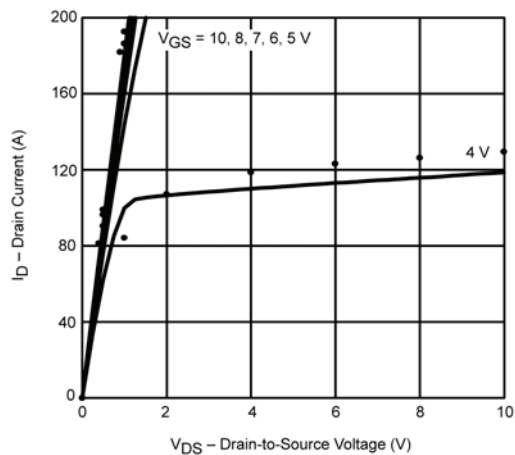
SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
<b>Static</b>					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	3.2	-	V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} > 5\ \text{V}$ , $V_{GS} = 10\ \text{V}$	637	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$ , $I_D = 30\ \text{A}$	0.0077	0.0078	$\Omega$
		$V_{GS} = 10\ \text{V}$ , $I_D = 30\ \text{A}$ , $T_J = 125^\circ\text{C}$	0.0120	-	
		$V_{GS} = 10\ \text{V}$ , $I_D = 30\ \text{A}$ , $T_J = 200^\circ\text{C}$	0.0160	-	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\ \text{V}$ , $I_D = 30\ \text{A}$	105	-	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 85\ \text{A}$ , $V_{GS} = 0\ \text{V}$	0.92	1	V
<b>Dynamic <sup>b</sup></b>					
Input Capacitance	$C_{iss}$	$V_{DS} = 25\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	6633	6700	pF
Output Capacitance	$C_{oss}$		701	750	
Reverse Transfer Capacitance	$C_{rss}$		254	280	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 50\ \text{V}$ , $V_{GS} = 10\ \text{V}$ , $I_D = 85\ \text{A}$	113	110	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$		24	24	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		24	24	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 50\ \text{V}$ , $R_L = 0.6\ \Omega$ $I_D = 85\ \text{A}$ , $V_{GEN} = 10\ \text{V}$ , $R_g = 2.5\ \Omega$	102	20	ns
Rise Time <sup>c</sup>	$t_r$		125	125	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$		124	55	
Fall Time <sup>c</sup>	$t_f$		138	130	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 50\ \text{A}$ , $dI/dt = 100\ \text{A}/\mu\text{s}$	85	70	

**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\ \%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.

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