Vishay Siliconix

N-Channel 80 V (D-S) MOSFET

DESCRIPTION

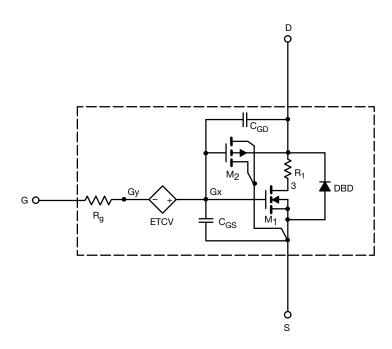
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to 125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.72	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	0.00704	0.00705	Ω
		V _{GS} = 4.5 V, I _D = 10 A	0.00997	0.00980	
Forward transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	40.6	37	S
Diode forward voltage	V _{SD}	$I_{S} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	0.75	0.77	V
Dynamic ^b					
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	2579	2070	pF
Output capacitance	C _{oss}		211.7	205	
Reverse transfer capacitance	C _{rss}		31.6	14	
Total gate charge	Qg	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A	32.9	32.5	nC
			15.7	15.2	
Gate-source charge	Q_{gs}	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	6.35	6.7	
Gate-drain charge	Q_{gd}		3.6	3.9	

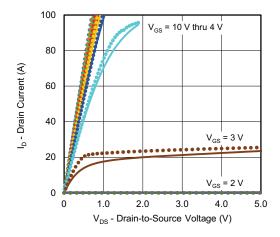
Notes

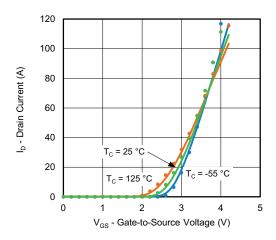
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

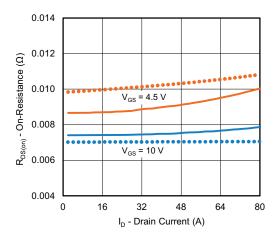
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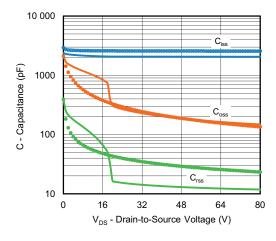
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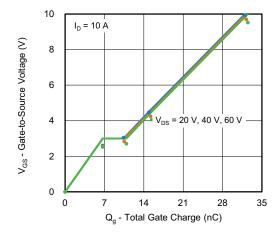
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

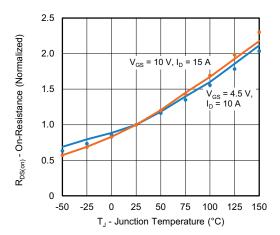












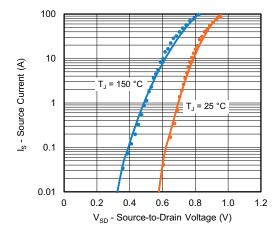
Note

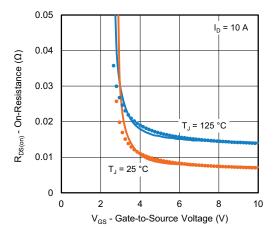
· Dots and squares represent measured data

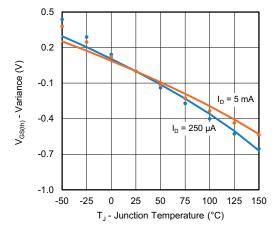
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COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25 \, ^{\circ}\text{C}$, unless otherwise noted)







Note

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