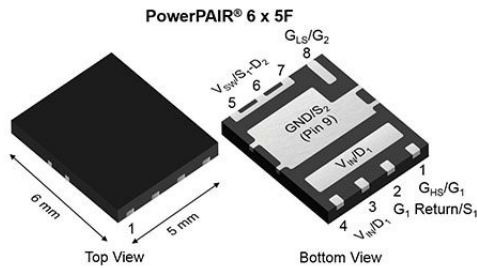


# Dual N-Channel 30 V (D-S) MOSFET With Schottky Diode



## FEATURES

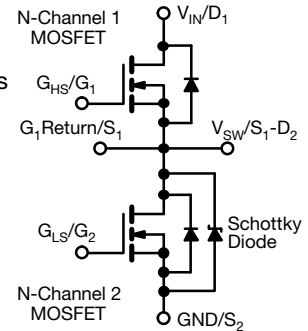
- TrenchFET® Gen IV power MOSFET
- SkyFET® low side MOSFET with integrated Schottky
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V <sub>DS</sub> (V)	30	30
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 10 V	0.0040	0.0019
R <sub>DS(on)</sub> max. (Ω) at V <sub>GS</sub> = 4.5 V	0.0067	0.0027
Q <sub>g</sub> typ. (nC)	7	17.3
I <sub>D</sub> (A) <sup>a</sup>	40	60
Configuration	Dual	

ORDERING INFORMATION	
Package	PowerPAIR 6 x 5F
Lead (Pb)-free and halogen-free	SiZF918DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage	V <sub>DS</sub>	30	30	V	
Gate-source voltage	V <sub>GS</sub>	+20, -16	+16, -12		
Continuous drain current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	40 <sup>a</sup>	60 <sup>a</sup>	
		T <sub>C</sub> = 70 °C	40 <sup>a</sup>	60 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	23 <sup>b, c</sup>	35 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	18.4 <sup>b, c</sup>	28 <sup>b, c</sup>	
Pulsed drain current (t = 100 μs)	I <sub>DM</sub>	130	100	A	
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	22		60 <sup>a</sup>
		T <sub>A</sub> = 25 °C	2.8 <sup>b, c</sup>		6.1 <sup>b, c</sup>
Single pulse avalanche current	I <sub>AS</sub>	15	18		
Single pulse avalanche energy	E <sub>AS</sub>	11.3	16	mJ	
Maximum power dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	26.6	50	
		T <sub>C</sub> = 70 °C	17	32	
		T <sub>A</sub> = 25 °C	3.4 <sup>b, c</sup>	3.7 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2.2 <sup>b, c</sup>	2.4 <sup>b, c</sup>	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150		°C	
Soldering recommendations (peak temperature) <sup>d, e</sup>		260			

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	CHANNEL-1		CHANNEL-2		UNIT	
		TYP.	MAX.	TYP.	MAX.		
Maximum junction-to-ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	30	37	27	34	°C/W
Maximum junction-to-case (source)	Steady state	R <sub>thJC</sub>	3.8	4.7	2	2.5	

## Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR 6 x 5F is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 77 °C/W for channel-1 and 70 °C/W for channel-2



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT		
<b>Static</b>								
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30	-	-	V	
			Ch-2	30	-	-		
Drain-source breakdown voltage (transient) <sup>c</sup>	$V_{DS(t)}$	$V_{GS} = 0\text{ V}, t_{(transient)} \leq 1\text{ }\mu\text{s}$	Ch-1	36	-	-		
			Ch-2	36	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.1	-	2.4		
			Ch-2	1.0	-	2.3		
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	Ch-1	-	-	$\pm 100$	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}, -12\text{ V}$	Ch-2	-	-	$\pm 100$		
Zero Gate voltage drain current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	-	1	$\mu\text{A}$	
			Ch-2	-	20	350		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1	-	-	5		
			Ch-2	-	200	3000		
On-state drain current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20	-	-	A	
			Ch-2	20	-	-		
Drain-source on-state resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	0.0029	0.0040	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	0.0012	0.0019		
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-1	-	0.0047	0.0068		
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-2	-	0.0018	0.0027		
Forward transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1	-	53	-	S	
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2	-	87	-		
<b>Dynamic <sup>a</sup></b>								
Input capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$  Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	1060	-	$\text{pF}$	
			Ch-2	-	2650	-		
Output capacitance	$C_{oss}$		Ch-1	-	600	-	$\text{pF}$	
			Ch-2	-	1240	-		
Reverse transfer capacitance	$C_{rss}$		Ch-1	-	45	-	$\text{pF}$	
			Ch-2	-	140	-		
$C_{rss}/C_{iss}$ ratio			Ch-1	-	0.042	0.085		
			Ch-2	-	0.053	0.106		
Total gate charge	$Q_g$		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	14.6	22	$\text{nC}$
			$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	37	56	
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	7	11		
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-2	-	17.4	27		
Gate-source charge	$Q_{gs}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	3	-	$\text{nC}$	
		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-2	-	6.1	-		
Gate-drain charge	$Q_{gd}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	1.5	-	$\text{nC}$	
		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-2	-	3.5	-		
Output charge	$Q_{oss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	14	-	$\text{nC}$	
			Ch-2	-	31	-		
Gate resistance	$R_g$	$f = 1\text{ MHz}$	Ch-1	0.2	1	2	$\Omega$	
			Ch-2	0.1	0.5	1		
Turn-on delay time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \equiv 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$  Channel-2 $V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \equiv 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	17	35	$\text{ns}$	
			Ch-2	-	22	45		
Rise time	$t_r$		Ch-1	-	45	90		
			Ch-2	-	55	110		
Turn-off delay time	$t_{d(off)}$		Ch-1	-	20	40		
			Ch-2	-	30	60		
Fall time	$t_f$		Ch-1	-	10	20		
			Ch-2	-	10	20		



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Dynamic <sup>a</sup></b>							
Turn-on delay time	t <sub>d(on)</sub>	Channel-1 V <sub>DD</sub> = 15 V, R <sub>L</sub> = 3 Ω I <sub>D</sub> ≅ 5 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	Ch-1	-	10	20	ns
Rise time	t <sub>r</sub>		Ch-2	-	15	30	
Turn-off delay time	t <sub>d(off)</sub>	Channel-2 V <sub>DD</sub> = 15 V, R <sub>L</sub> = 3 Ω I <sub>D</sub> ≅ 5 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	Ch-1	-	5	10	
			Ch-2	-	26	50	
Fall time	t <sub>f</sub>		Ch-1	-	20	40	
			Ch-2	-	30	60	
			Ch-1	-	5	10	
			Ch-2	-	5	10	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	Ch-1	-	-	22	A
			Ch-2	-	-	60	
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>		Ch-1	-	-	130	
			Ch-2	-	-	100	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V	Ch-1	-	0.8	1.2	V
		I <sub>S</sub> = 3 A, V <sub>GS</sub> = 0 V	Ch-2	-	0.4	0.6	
Body diode reverse recovery time	t <sub>rr</sub>	Channel-1 I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	Ch-1	-	32	70	ns
			Ch-2	-	55	110	
Body diode reverse recovery charge	Q <sub>rr</sub>	Channel-2 I <sub>F</sub> = 5 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	Ch-1	-	24	50	nC
			Ch-2	-	66	135	
Reverse recovery fall time	t <sub>a</sub>		Ch-1	-	18	-	ns
			Ch-2	-	27	-	
Reverse recovery rise time	t <sub>b</sub>		Ch-1	-	14	-	
			Ch-2	-	28	-	

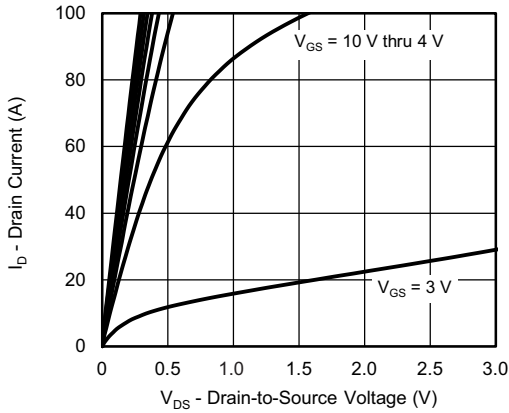
**Notes**

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- c. Based on characterization, not subject to production testing

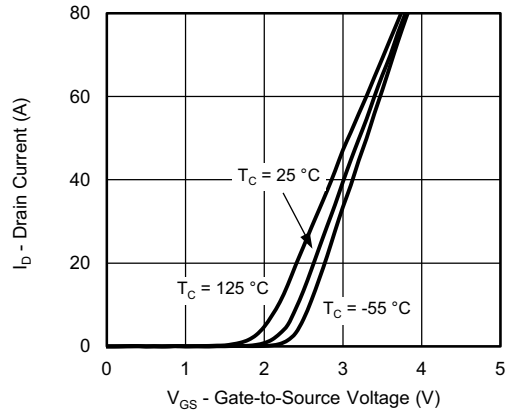
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



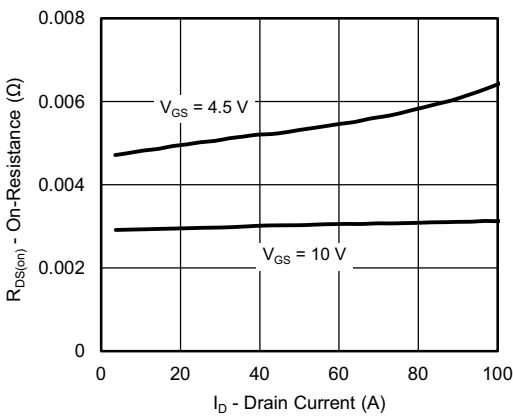
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



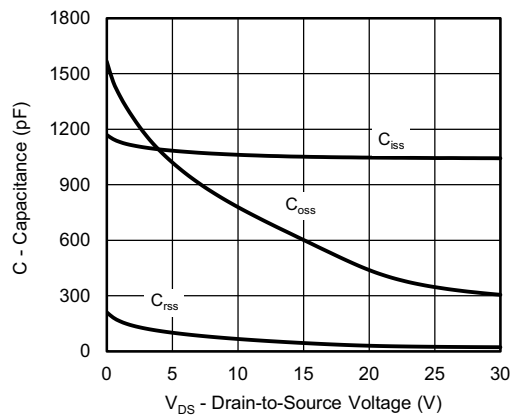
Output Characteristics



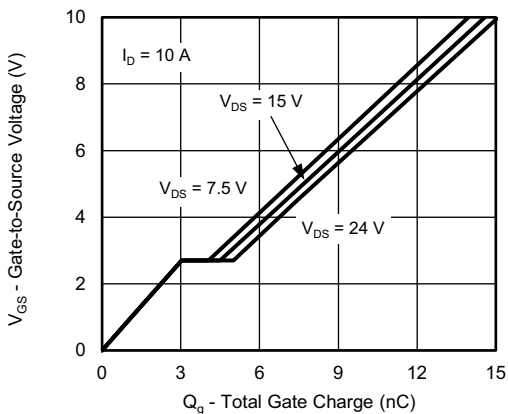
Transfer Characteristics



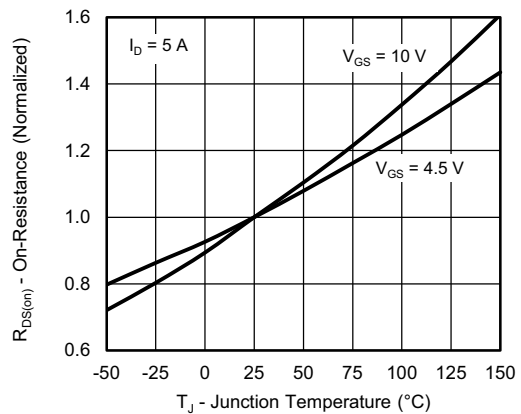
On-Resistance vs. Drain Current



Capacitance

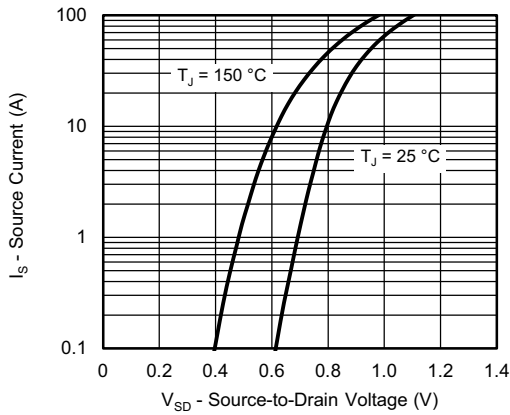


Gate Charge

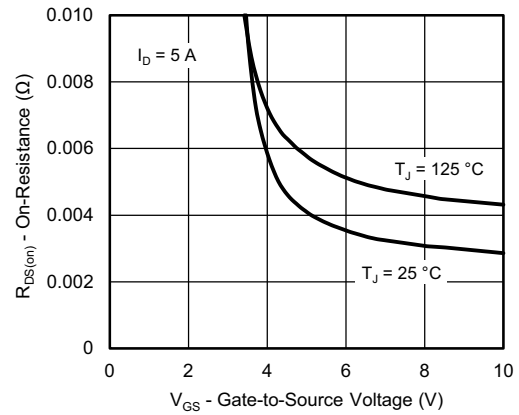


On-Resistance vs. Junction Temperature

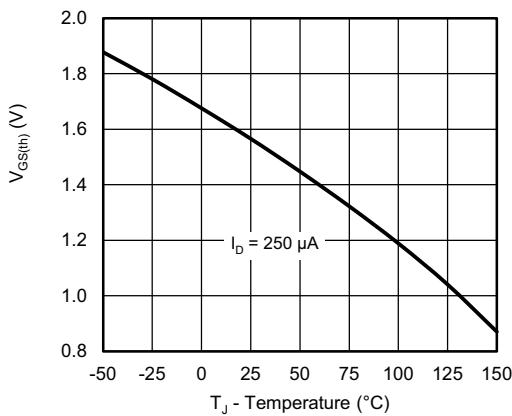
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



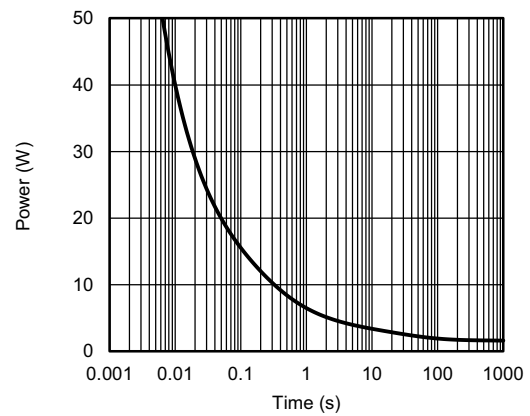
**Source-Drain Diode Forward Voltage**



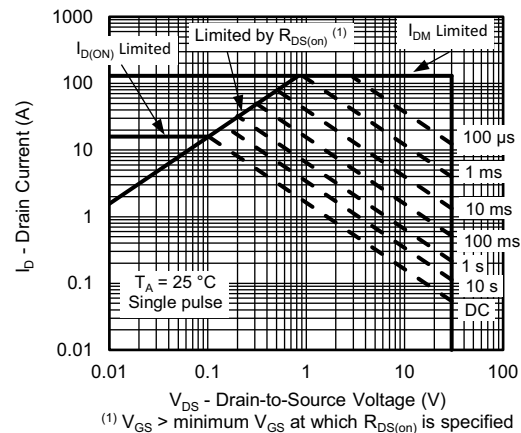
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



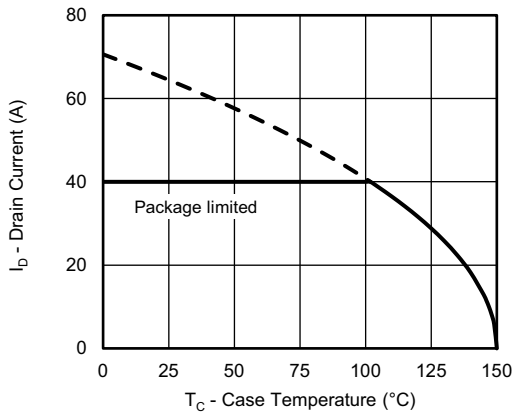
**Single Pulse Power, Junction-to-Ambient**



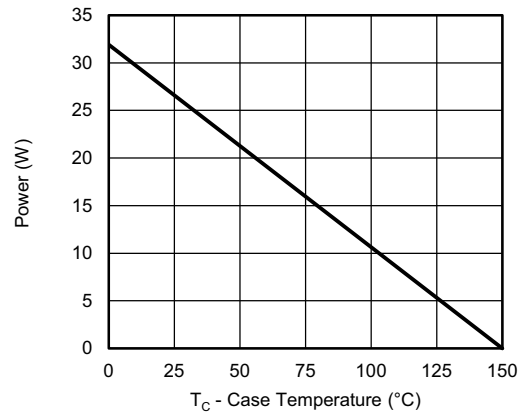
**Safe Operating Area, Junction-to-Ambient**



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**

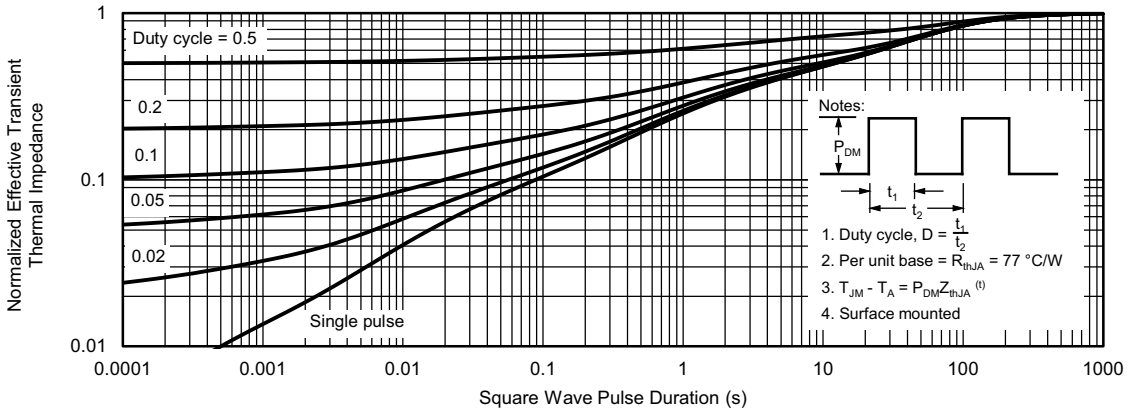


**Power, Junction-to-Case**

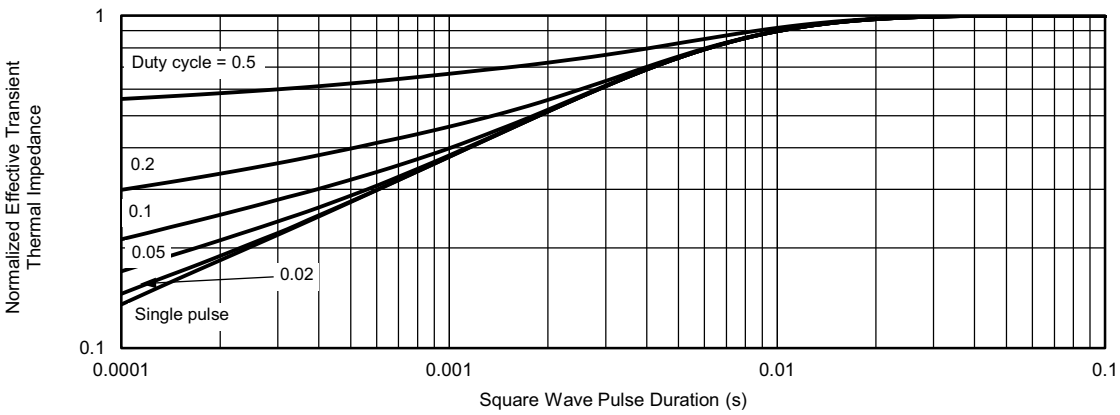
**Note**

- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

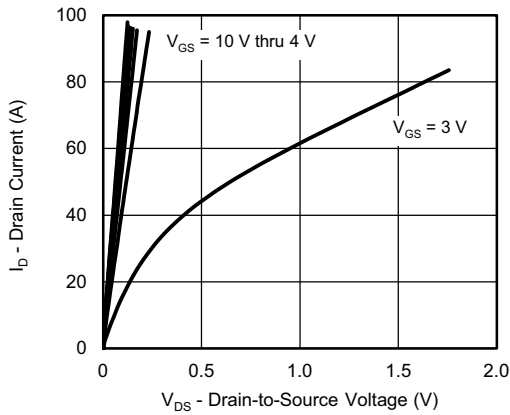


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

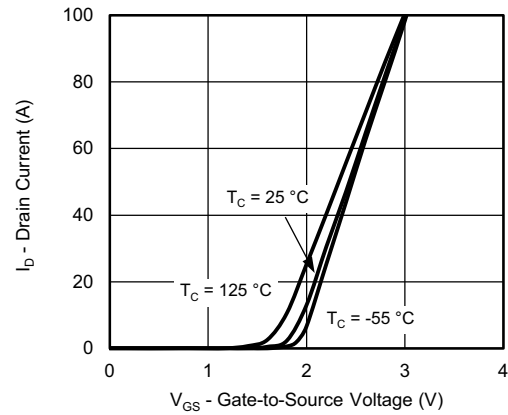


**Normalized Thermal Transient Impedance, Junction-to-Case**

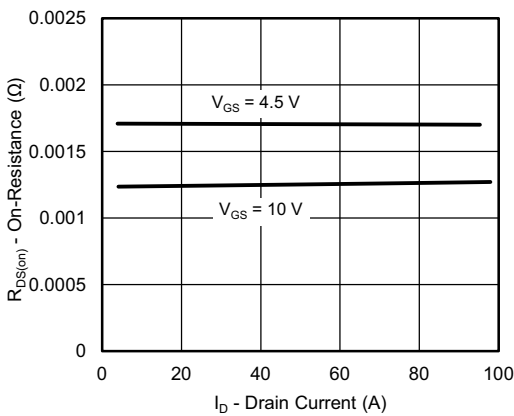
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



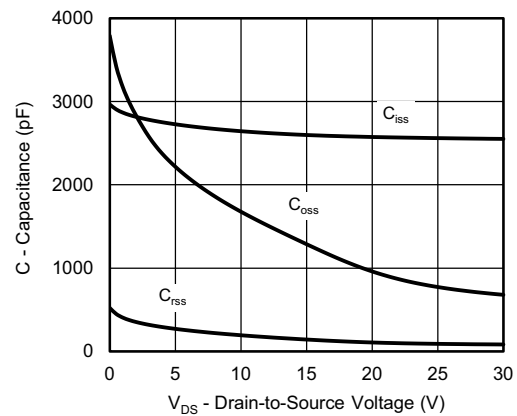
**Output Characteristics**



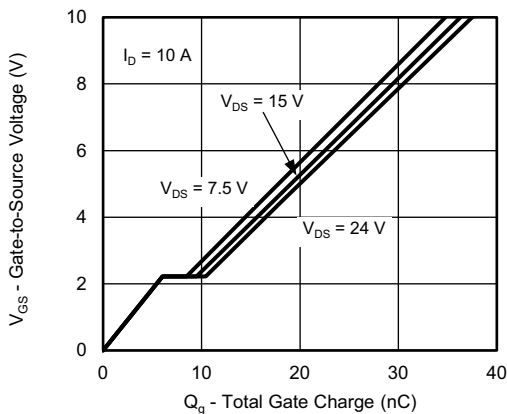
**Transfer Characteristics**



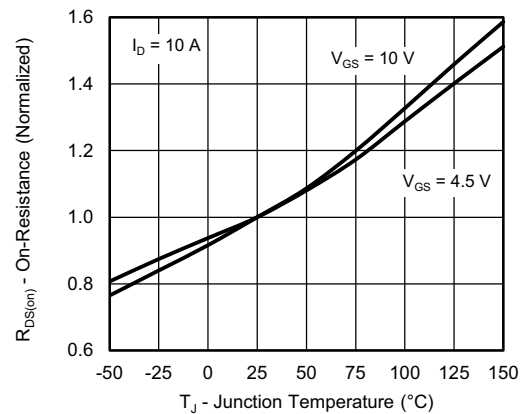
**On-Resistance vs. Drain Current**



**Capacitance**



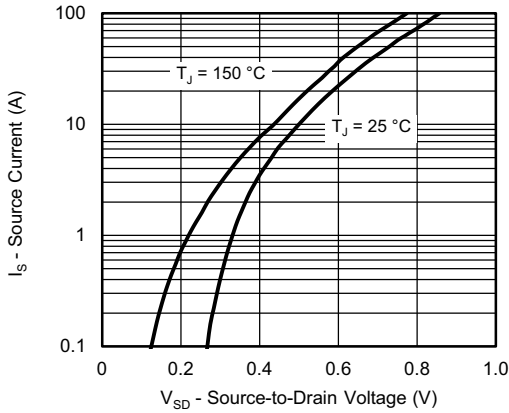
**Gate Charge**



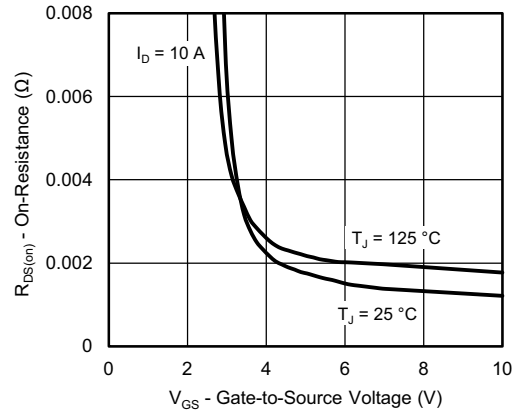
**On-Resistance vs. Junction Temperature**



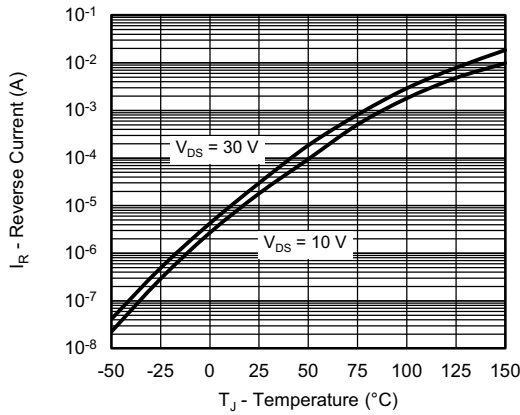
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



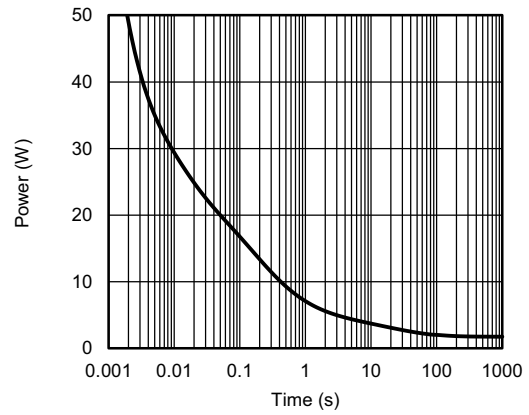
**Source-Drain Diode Forward Voltage**



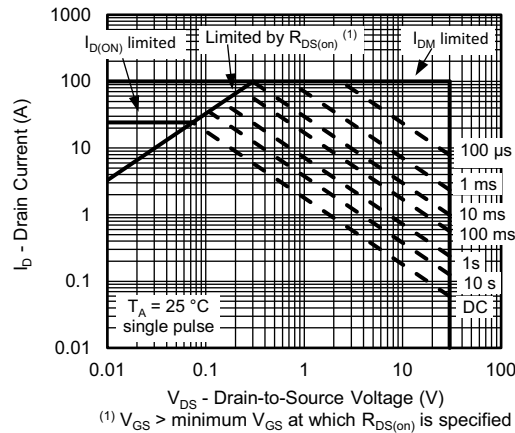
**On-Resistance vs. Gate-to-Source Voltage**



**Reverse Current (Schottky)**



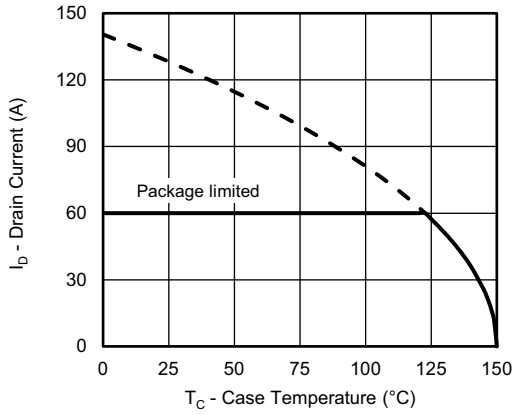
**Single Pulse Power, Junction-to-Ambient**



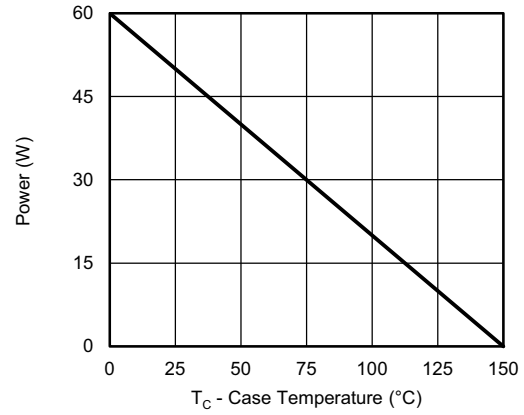
**Safe Operating Area, Junction-to-Ambient**



**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



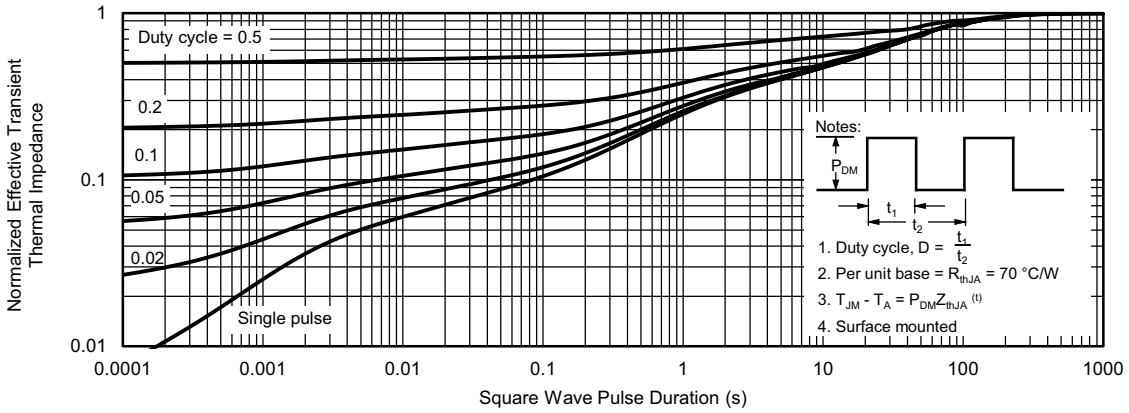
**Power, Junction-to-Case**

**Note**

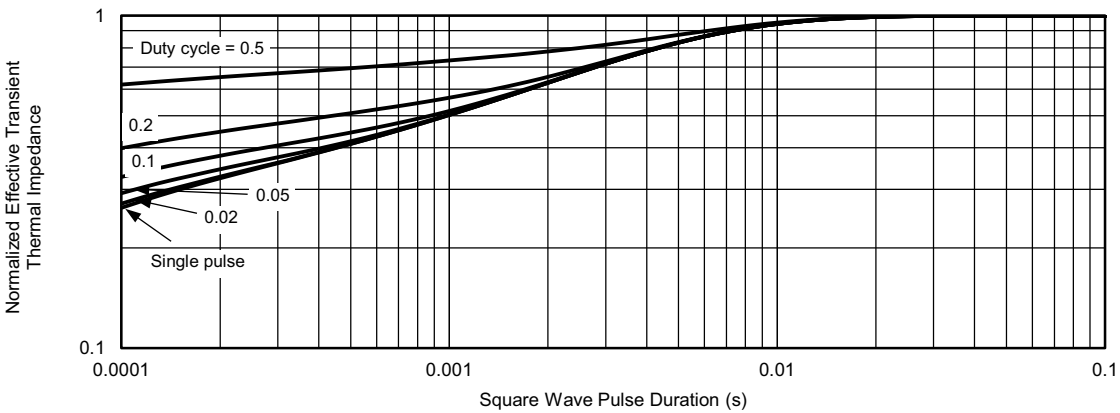
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75963](http://www.vishay.com/ppg?75963).

### PowerPAIR® 6 x 5 F Case Outline

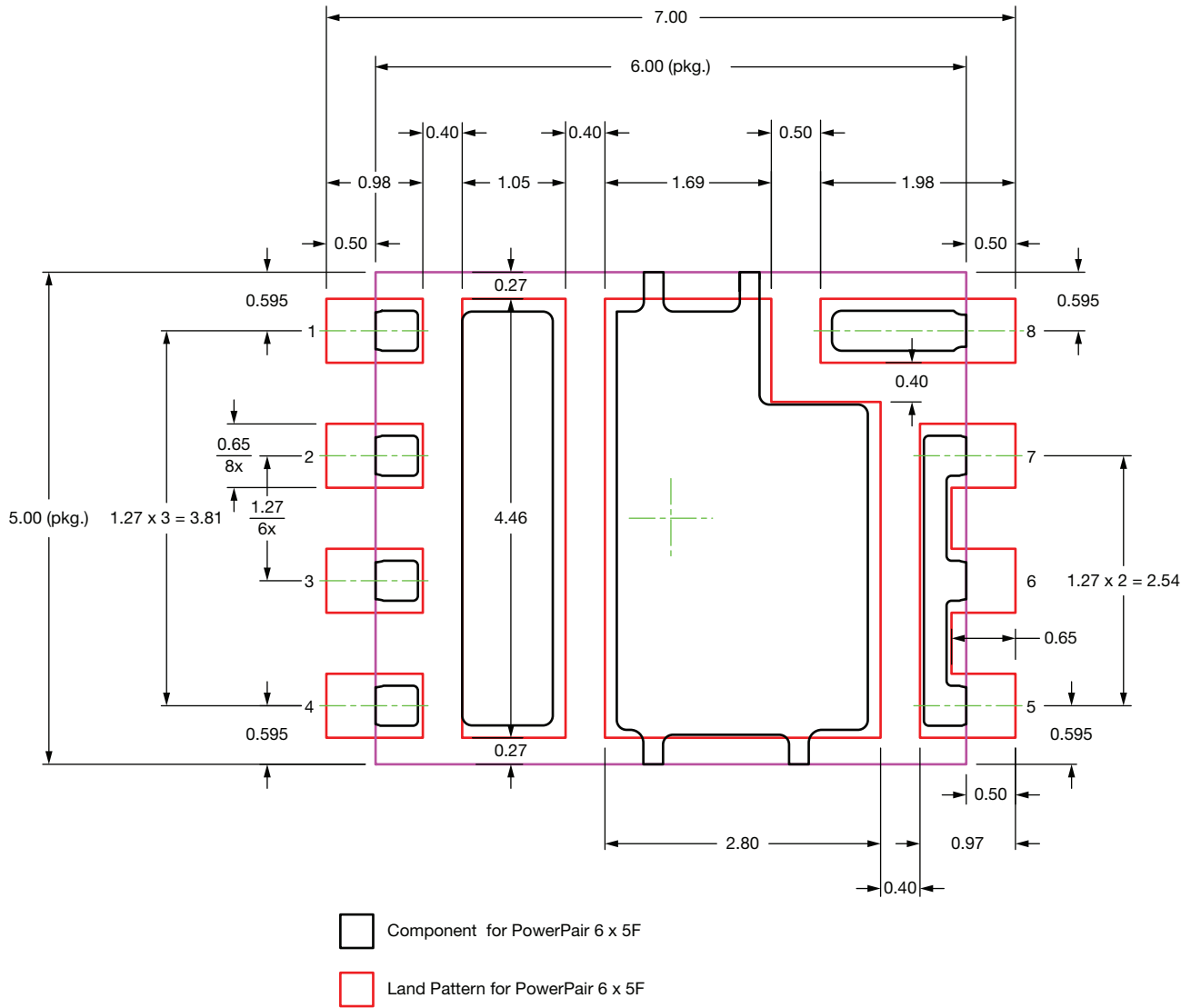


DIMENSION	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.10	0.000	-	0.004
b	0.35	0.41	0.46	0.014	0.016	0.018
b1	0.38 ref.			0.015 ref.		
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.26	3.31	3.36	0.128	0.130	0.132
D2	4.20	4.30	4.40	0.165	0.169	0.173
D3	4.15	4.20	4.25	0.163	0.165	0.167
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	2.50	2.55	2.60	0.098	0.100	0.102
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
e1	3.81 BSC			0.150 BSC		
K	0.52	0.57	0.62	0.020	0.022	0.024
K1	0.69	0.74	0.79	0.027	0.029	0.031
K2	0.60	0.65	0.70	0.024	0.026	0.028
K3	0.39 BSC			0.015 BSC		
K4	0.50	0.55	0.60	0.020	0.022	0.024
K5	0.25	0.30	0.35	0.010	0.012	0.014
K6	0.40	0.45	0.50	0.016	0.018	0.020
K7	0.35	0.40	0.45	0.014	0.016	0.018
K8	0.30	0.35	0.40	0.012	0.014	0.016
L	0.33	0.43	0.53	0.013	0.017	0.021
L1	1.31	1.36	1.41	0.052	0.054	0.056
L2	0.20 ref.			0.008 ref.		
ECN: T20-0097-Rev. C, 25-Feb-2020						
DWG: 6043						

#### Note

- Millimeters will govern

**Recommended Minimum PADs for PowerPAIR® 6 x 5F**



**Note**

- Dimensions in millimeters



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