

## N-Channel 60 V (D-S) MOSFET

### DESCRIPTION

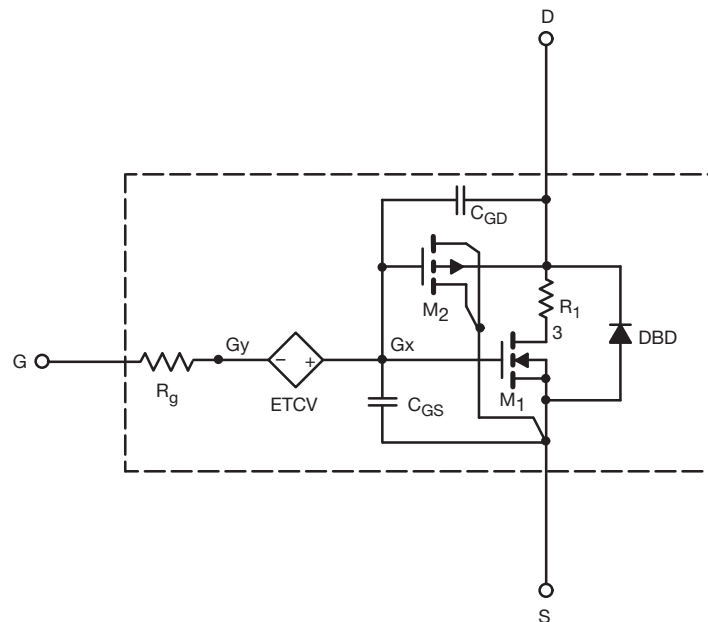
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



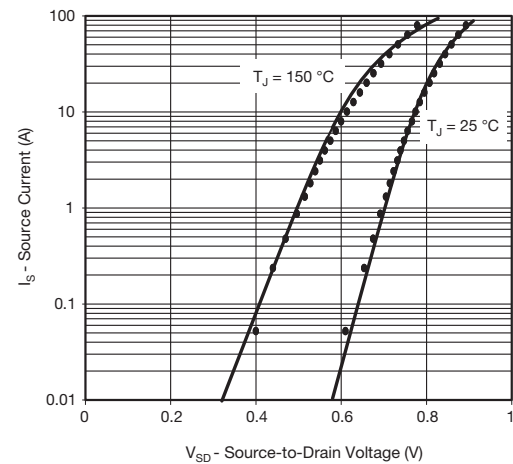
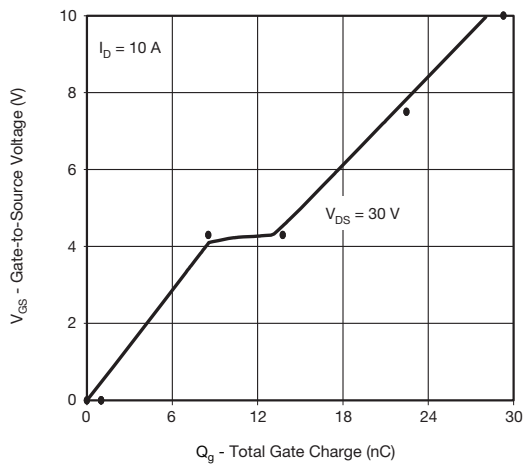
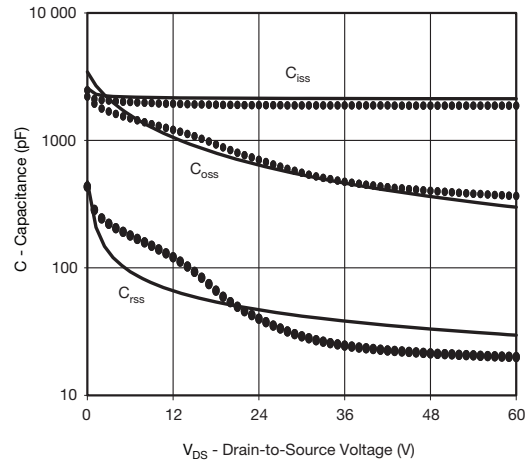
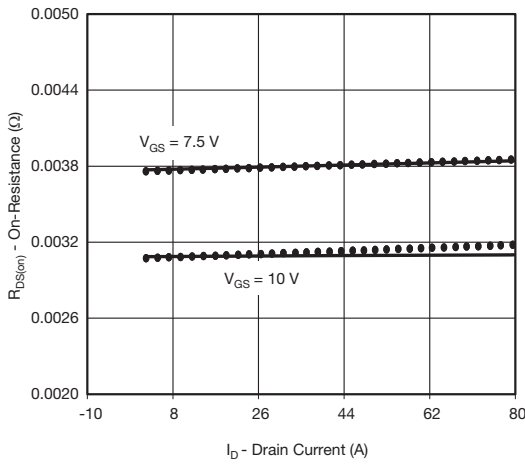
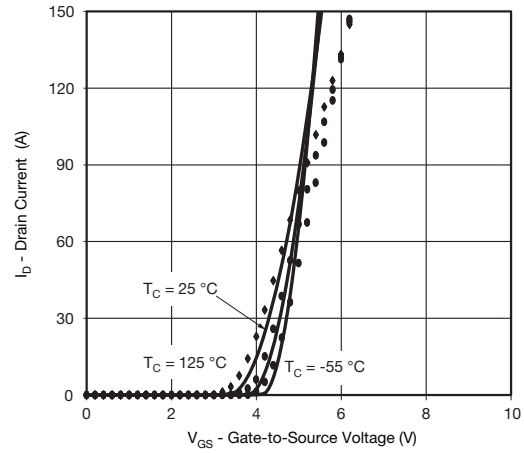
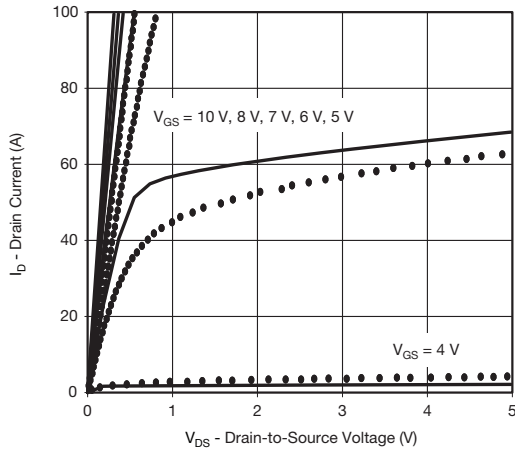
| <b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |              |   |                |               |          |
|--|--------------|---|----------------|---------------|----------|
| PARAMETER  | SYMBOL       | TEST CONDITIONS   | SIMULATED DATA | MEASURED DATA | UNIT     |
| <b>Static</b>  |              |   |                |               |          |
| Gate-source threshold voltage  | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$                           | 2.8            | -             | V        |
| Drain-source on-state resistance <sup>a</sup>                                      | $R_{DS(on)}$ | $V_{GS} = 10\ \text{V}, I_D = 15\ \text{A}$                         | 0.00310        | 0.00325       | $\Omega$ |
|  |              | $V_{GS} = 7.5\ \text{V}, I_D = 10\ \text{A}$                        | 0.00380        | 0.00385       |          |
| Forward transconductance <sup>a</sup>  | $g_{fs}$     | $V_{DS} = 15\ \text{V}, I_D = 15\ \text{A}$                         | 54             | 50            | S        |
| Diode forward voltage  | $V_{SD}$     | $I_S = 5\ \text{A}$   | 0.75           | 0.77          | V        |
| <b>Dynamic <sup>b</sup></b>  |              |   |                |               |          |
| Input capacitance  | $C_{iss}$    | $V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$    | 2140           | 1870          | pF       |
| Output capacitance   | $C_{oss}$    |   | 537            | 565           |          |
| Reverse transfer capacitance   | $C_{rss}$    |   | 42             | 29            |          |
| Total gate charge  | $Q_g$        | $V_{DS} = 30\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 10\ \text{A}$  | 28             | 28.8          | nC       |
|  |              | $V_{DS} = 30\ \text{V}, V_{GS} = 7.5\ \text{V}, I_D = 10\ \text{A}$ | 22             | 22.5          |          |
| Gate-source charge   | $Q_{gs}$     |   | 8.7            | 8.7           |          |
| Gate-drain charge  | $Q_{gd}$     |   | 5              | 5.1           |          |

**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\ \%$   
b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data

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