SPICE Device Model SiSH617DN



Vishay Siliconix

P-Channel 30 V (D-S) MOSFET

DESCRIPTION

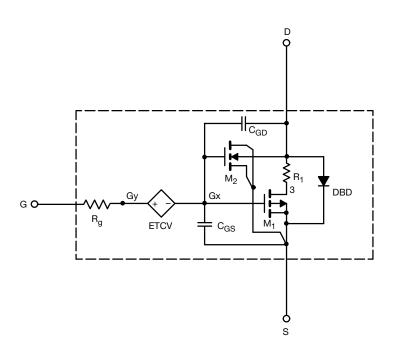
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	1.4	-	V
Drain-source on-state resistance ^a	Б	$V_{GS} = -10 \text{ V}, \text{ I}_{D} = -13.9 \text{ A}$	0.0107	0.0103	Ω
	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -10.3 \text{ A}$	0.0187	0.0185	
Forward transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -13.9 A	29	35	S
Diode forward voltage	V _{SD}	I _S = -11.1 A	-0.8	-0.8	V
Dynamic ^b		•			
Input capacitance	C _{iss}	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz	1780	1800	pF
Output capacitance	C _{oss}		372	370	
Reverse transfer capacitance	C _{rss}		257	312	
Total gate charge		$V_{DS} = -15 \text{ V}, \text{ V}_{GS} = -10 \text{ V}, \text{ I}_{D} = -13.9 \text{ A}$	38	39	nC
	Qg	$V_{DS} = -15 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -13.9 \text{ A}$	20	20.5	
Gate-source charge	Q _{gs}		6	6	
Gate-drain charge	Q _{gd}		11	11	

Notes

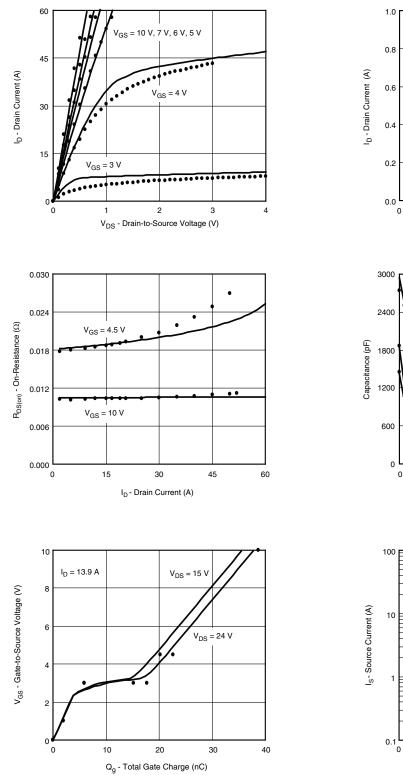
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %

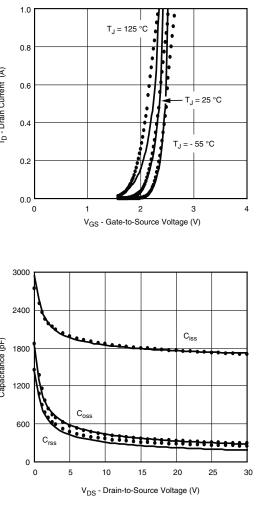
b. Guaranteed by design, not subject to production testing

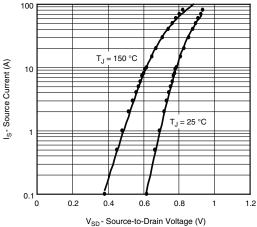


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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)







Note

• Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.

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