Automotive P-Channel 40 V (D-S) 175 °C MOSFET

DESCRIPTION

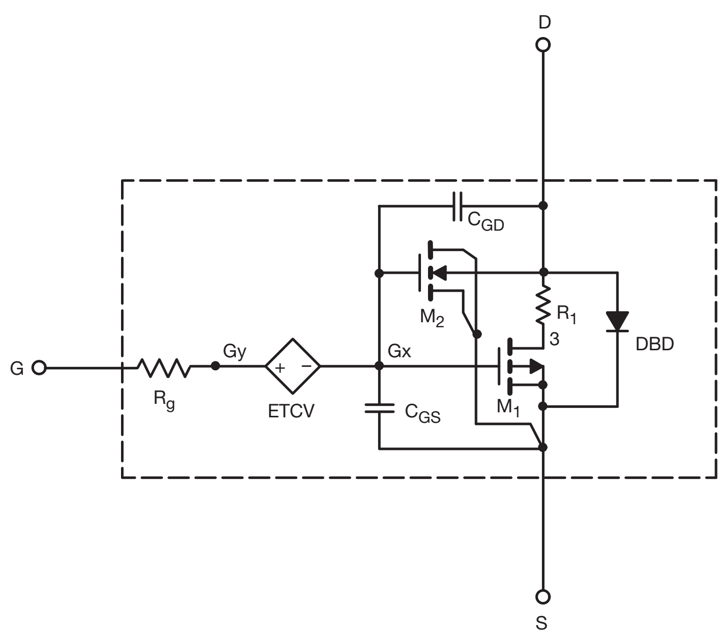
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

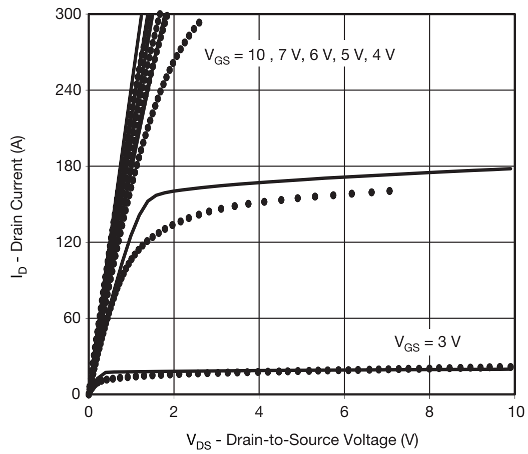
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = -250 μA	2	-	V
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -30 A	0.0042	0.0042	Ω
		V_{GS} = -4.5 V, I_D = -25 A	0.0059	0.0059	
Forward transconductance [a]	g_{fs}	V_{DS} = -30 V, I_D = -15 A	76	103	S
Diode forward voltage	V_{SD}	I_S = -30 A	-0.83	-0.84	V
Dynamic [b]					
Input capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	12 100	11 063	pF
Output capacitance	C_{oss}		826	847	
Reverse transfer capacitance	C_{rss}		819	757	
Total gate charge	Q_g	V_{DS} = -20 V, V_{GS} = -10 V, I_D = -50 A	180	185	nC
Gate-source charge	Q_{gs}		36	25	
Gate-drain charge	Q_{gd}		36	30	

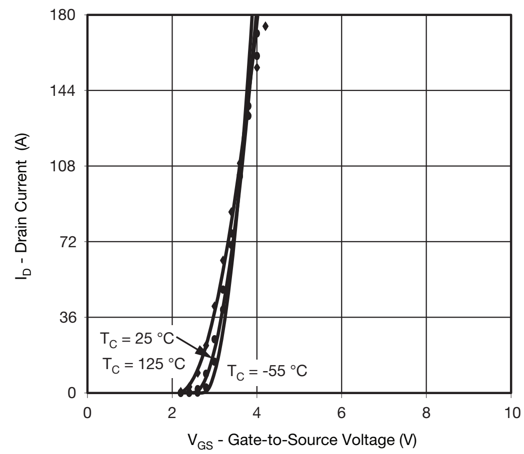
Notes

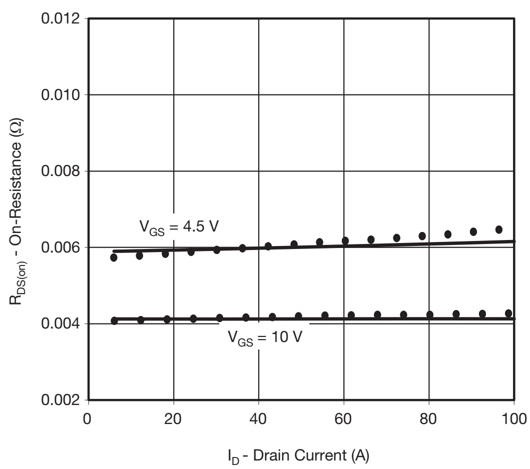
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

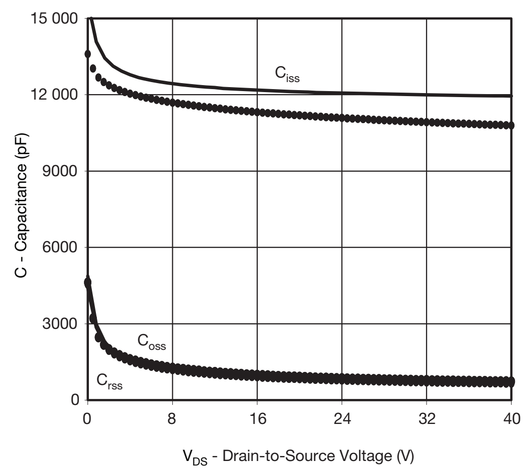
b. Guaranteed by design, not subject to production testing

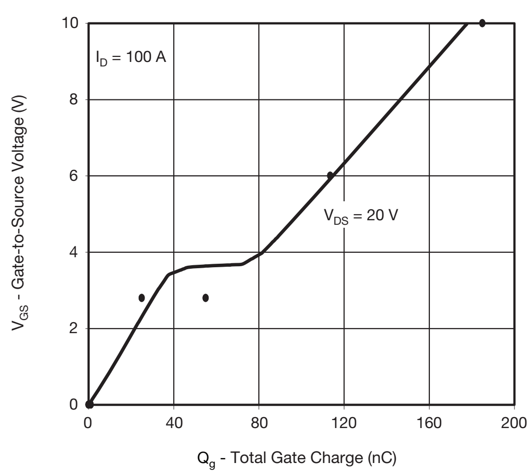
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

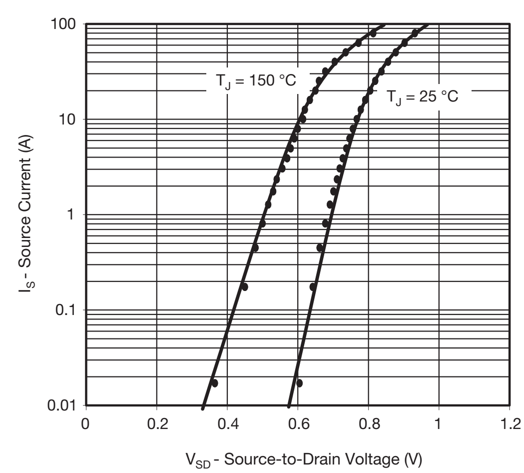












Note

- Dots and squares represent measured data

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