

## Automotive N- and P-Channel 60 V (D-S) 175 °C MOSFET

### DESCRIPTION

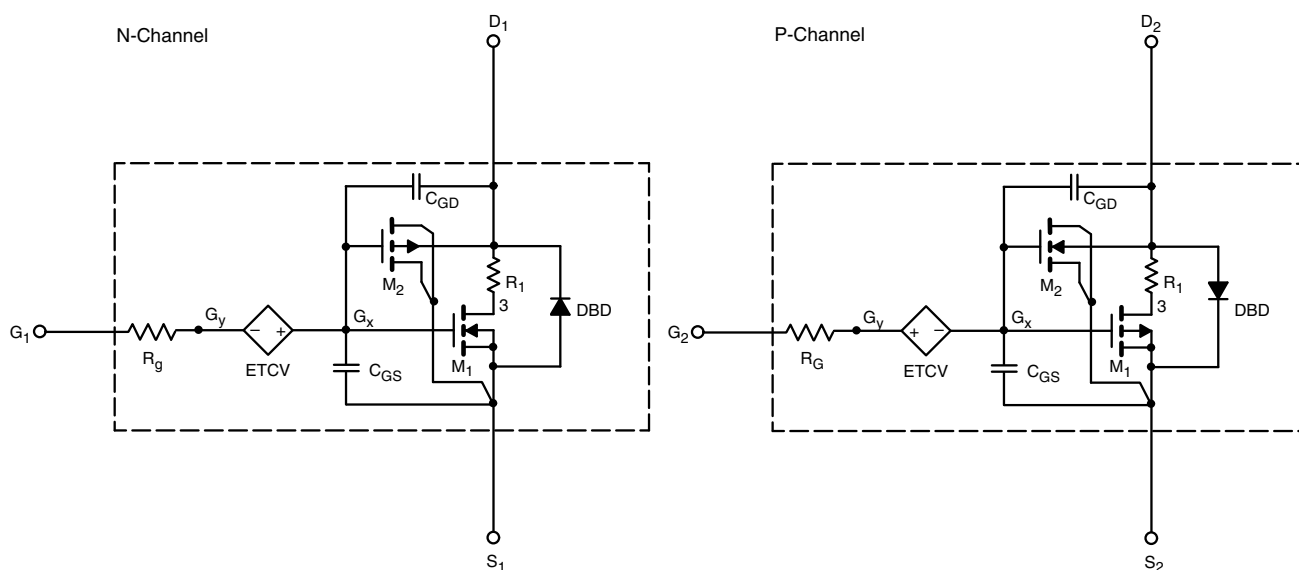
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N- and P-Channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	2	2	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	2	2	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	N-Ch	0.0105	0.0099	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A	P-Ch	0.0436	0.0432	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 8 A	N-Ch	0.0135	0.0133	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -8 A	P-Ch	0.0639	0.0628	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	N-Ch	45	56	S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 A	P-Ch	16	16	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 10 A	N-Ch	0.82	0.83	V
		I <sub>S</sub> = -10 A	P-Ch	-0.86	-0.88	
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz  P-Channel V <sub>DS</sub> = -25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch	1340	1205	pF
Output Capacitance	C <sub>oss</sub>		P-Ch	1270	1195	
			N-Ch	554	560	
Reverse Transfer Capacitance	C <sub>rss</sub>		P-Ch	162	162	
			N-Ch	30	29	
			P-Ch	103	102	
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A  P-Channel V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A	N-Ch	17	18	nC
Gate-Source Charge	Q <sub>gs</sub>		P-Ch	26	29	
			N-Ch	4	4	
Gate-Drain Charge	Q <sub>gd</sub>		P-Ch	4	5	
			N-Ch	2	2	
			P-Ch	7	7	

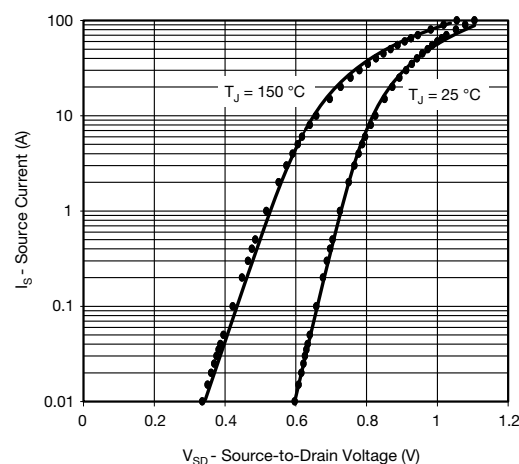
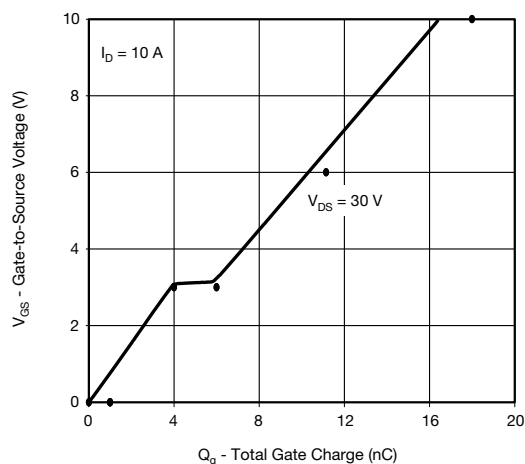
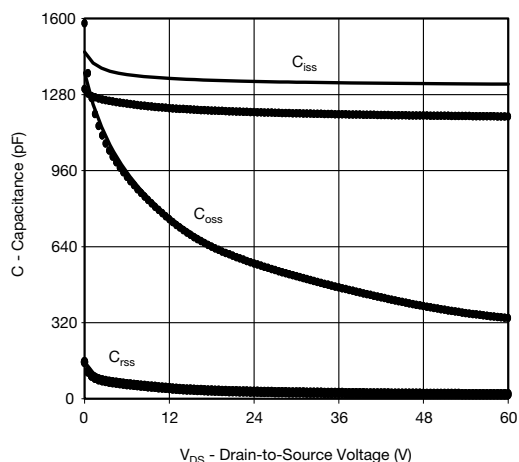
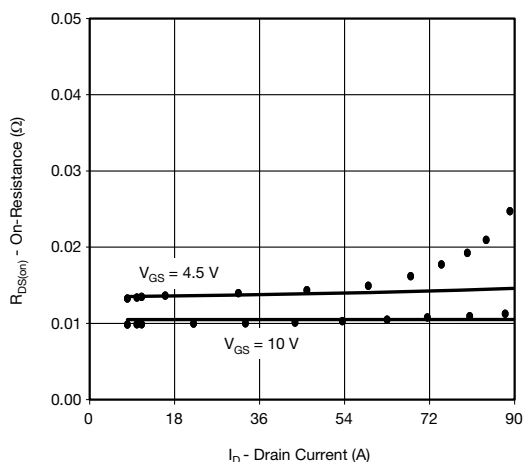
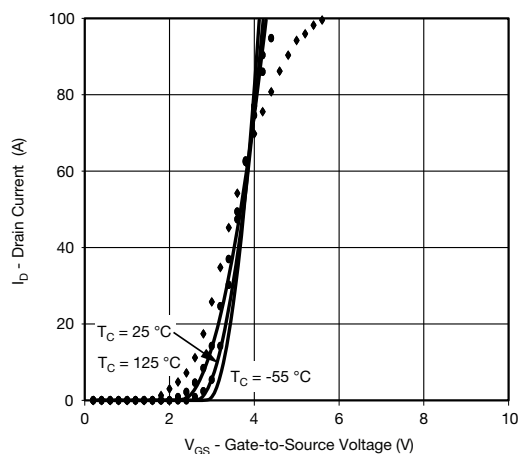
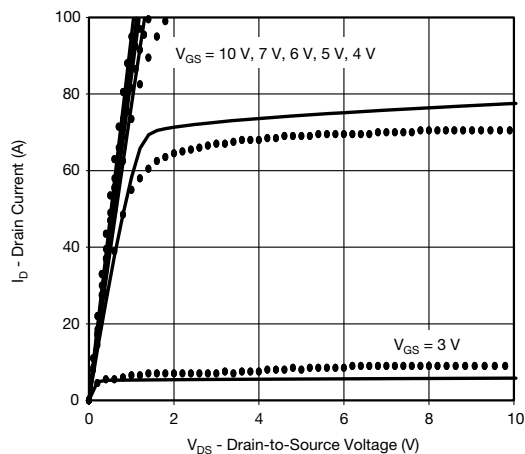
**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\ \%$   
b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

### N-Channel MOSFET



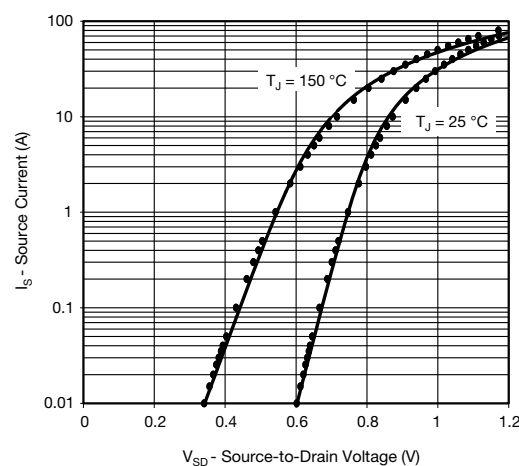
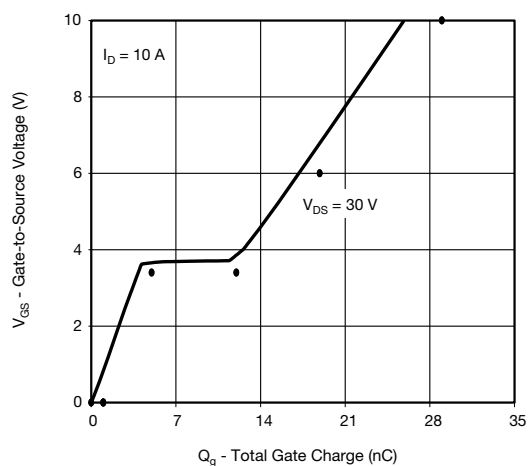
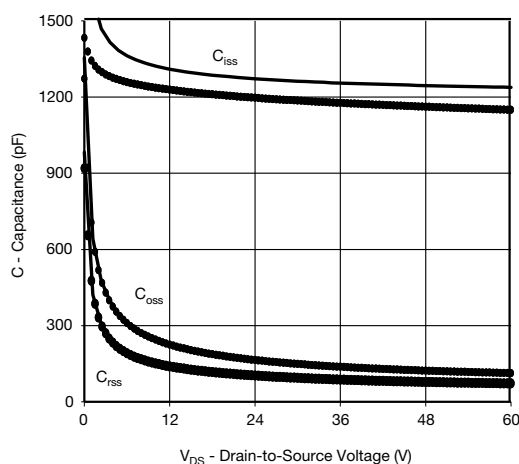
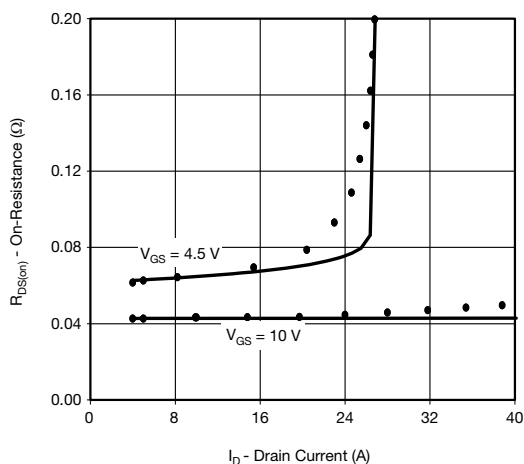
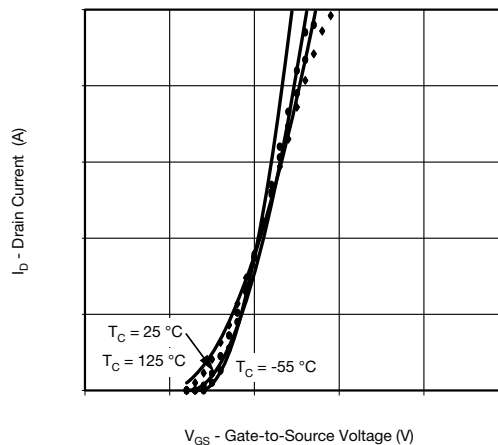
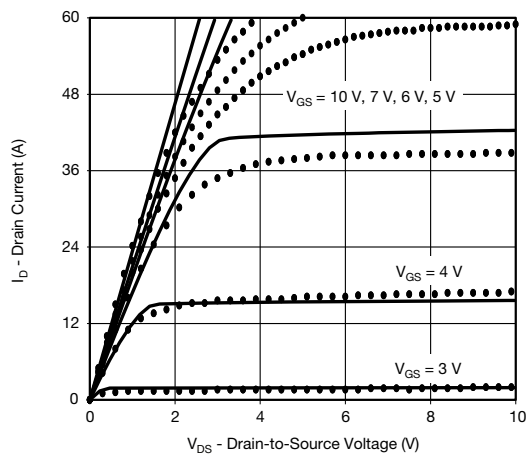
### Note

- Dots and squares represent measured data.



## COMPARISON OF MODEL WITH MEASURED DATA $T_J = 25^\circ\text{C}$ , unless otherwise noted

### P-Channel MOSFET



### Note

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