

## P-Channel 20 V (D-S) MOSFET

### DESCRIPTION

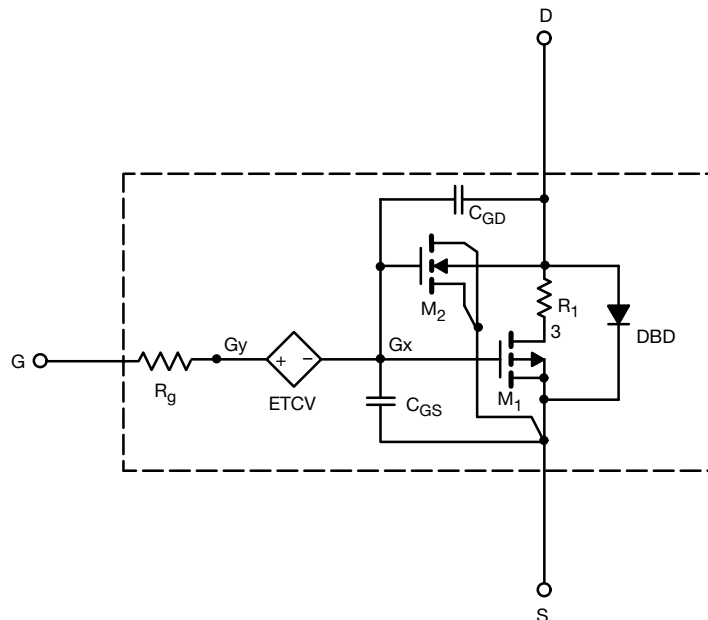
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



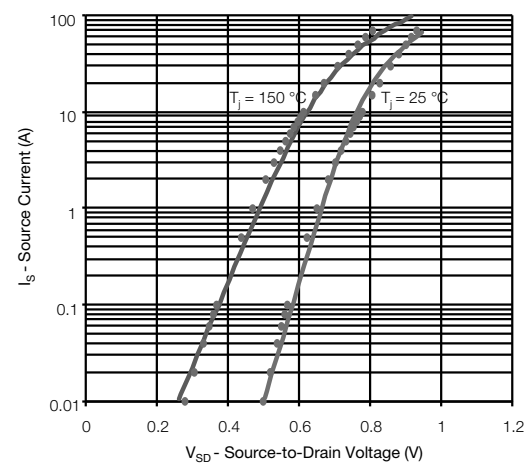
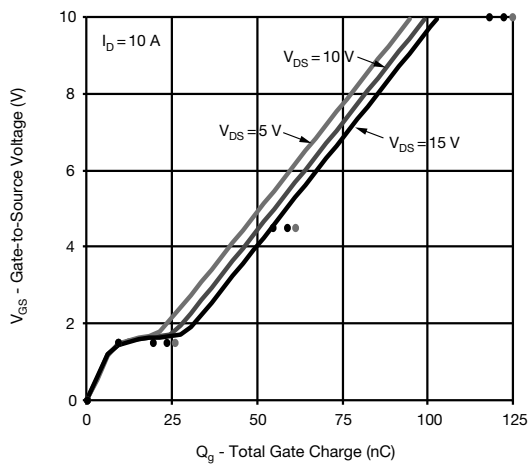
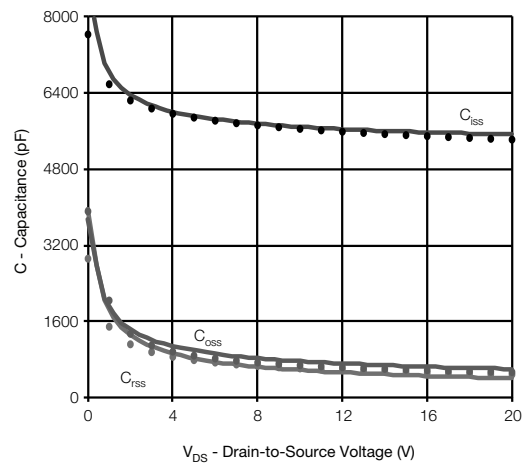
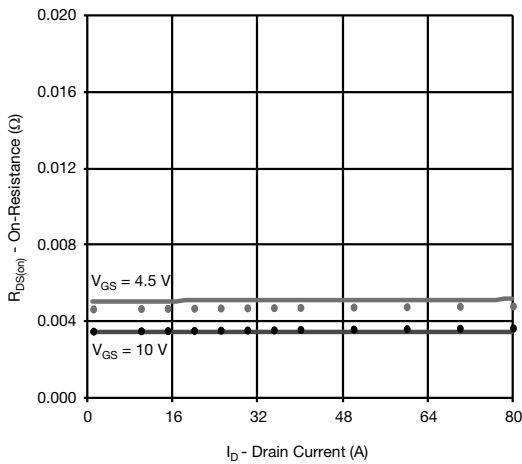
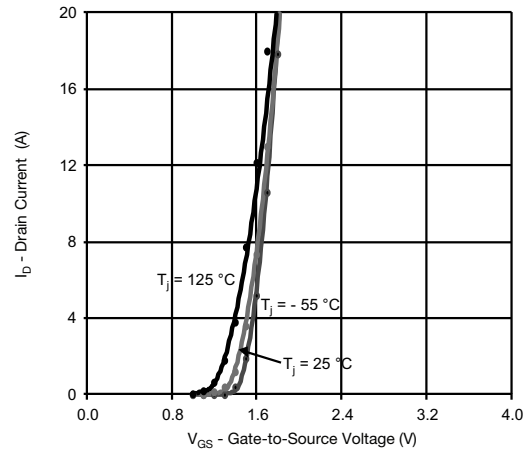
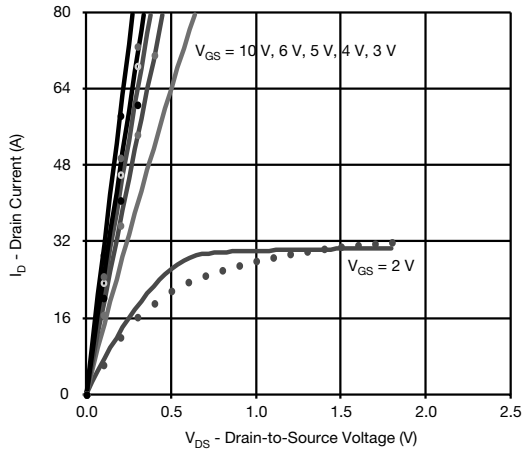
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
<b>Static</b>					
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	0.9	-	V
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -20\text{ A}$	0.0035	0.0035	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -15\text{ A}$	0.0050	0.0047	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -20\text{ A}$	72	82	S
Diode forward voltage	$V_{SD}$	$I_S = -4\text{ A}$	-0.72	-0.72	V
<b>Dynamic <sup>b</sup></b>					
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	5690	5590	pF
Output capacitance	$C_{oss}$		582	640	
Reverse transfer capacitance	$C_{rss}$		765	706	
Total gate charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$	101	122	nC
		$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$	52	59	
Gate-source charge	$Q_{gs}$		9.1	9.1	
Gate-drain charge	$Q_{gd}$		14.2	14.2	

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\text{ }\%$
- b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data

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