

## N-Channel 60 V (D-S) MOSFET

### DESCRIPTION

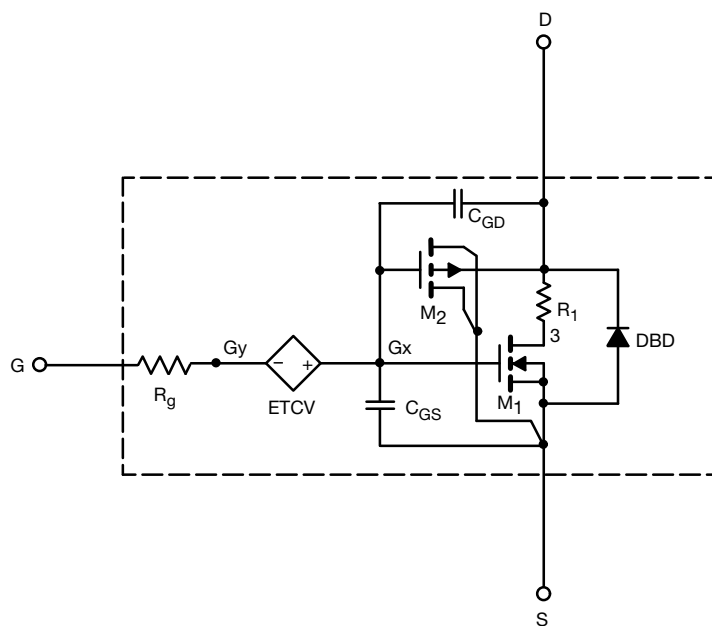
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +150 °C temperature ranges under the pulsed -20 V to +20 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel TrenchFET® gen IV power MOSFET
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +150 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



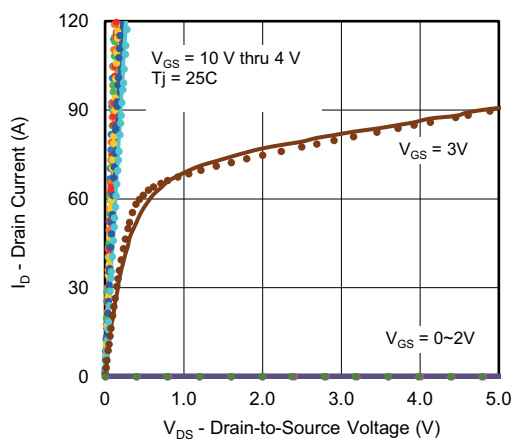
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.8	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 25 °C	0.00096	0.0012	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 25 °C	0.0018	0.0017	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 150 °C	0.00178	-	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	144	140	S
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	5720	5900	pF
Output capacitance	C <sub>oss</sub>		1281	1340	
Reverse transfer capacitance	C <sub>rss</sub>		55	60	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	95	89	nC
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	43	41	
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	15.3	17.4	
Gate-drain charge	Q <sub>gd</sub>		10.3	10.8	
Drain-Source Body Diode Characteristics					
Body diode voltage	V <sub>SD</sub>	I <sub>F</sub> = 5 A, V <sub>GS</sub> = 0 V	0.71	0.71	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, V <sub>DD</sub> = 25 V di/dt = 100 A/μs	56	54	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		64	70	nC
Reverse recovery fall time	t <sub>a</sub>		24	27	ns
Reverse recovery rise time	t <sub>b</sub>		32	27	
Reverse peak current	I <sub>rm</sub>			2.3	-

**Notes**

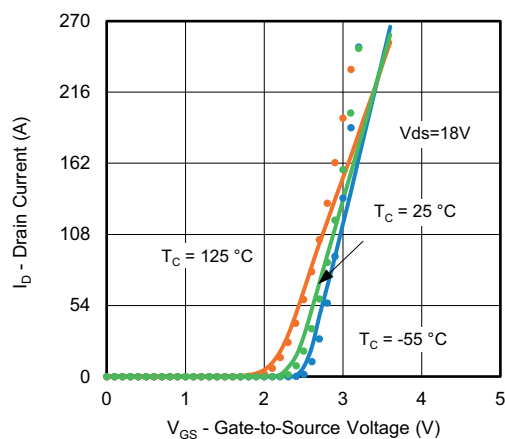
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing



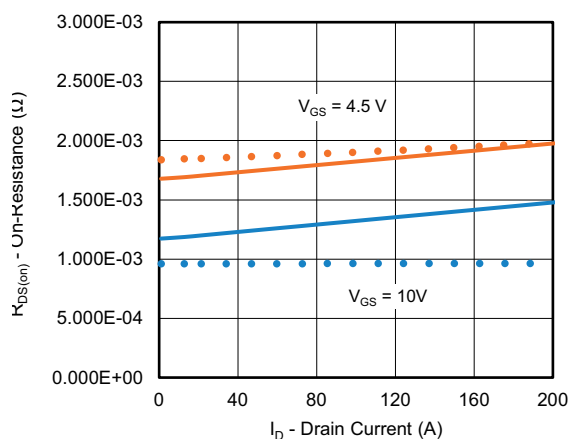
## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



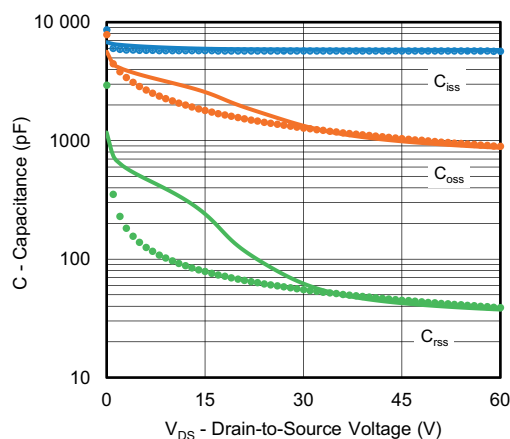
Output Characteristics



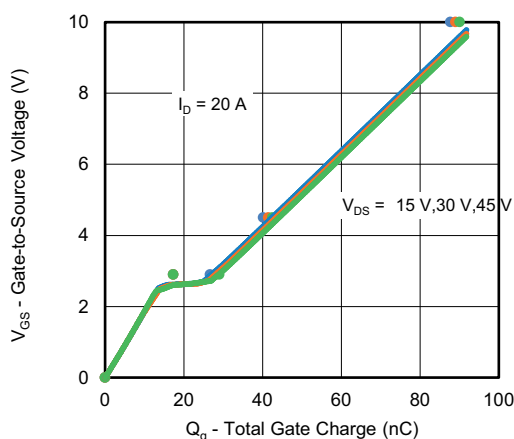
Transfer Characteristics



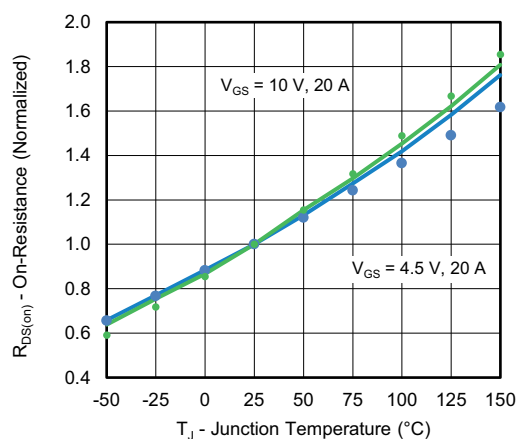
On-Resistance vs. Drain Current (A)



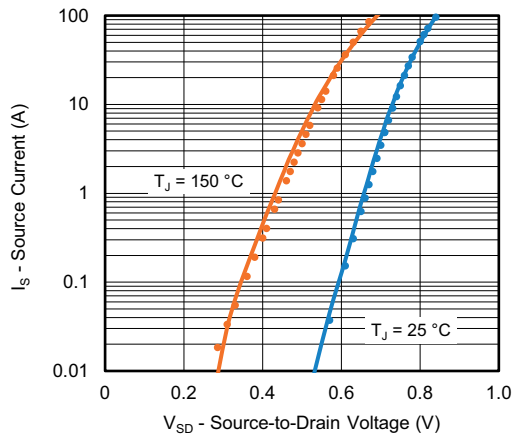
Capacitance



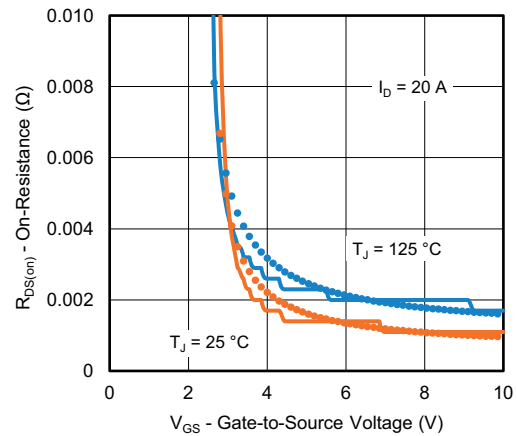
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

**Note**

- Dots and squares represent measured data

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