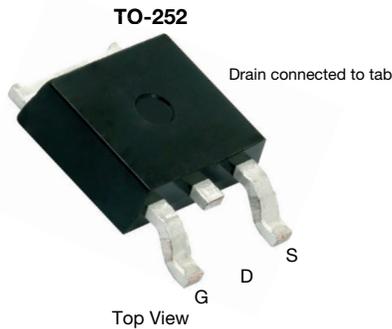


N-Channel 150 V (D-S) 175 °C MOSFET



FEATURES

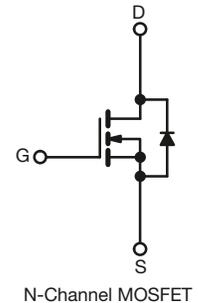
- ThunderFET® power MOSFET
- Maximum 175 °C junction temperature
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Boost converter
- LED backlighting
- Synchronous rectification
- Power supplies
- DC/AC inverter



PRODUCT SUMMARY	
V _{DS} (V)	150
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0447
Q _g typ. (nC)	10.5
I _D (A)	42 ^d
Configuration	Single

ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and halogen-free	SUD80460E-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	150	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current	T _C = 25 °C	I _D	42 ^d	A
	T _C = 125 °C		18.1	
Pulsed drain current (t = 100 μs)		I _{DM}	40	
Continuous source-drain diode current		I _S	42 ^d	
Single pulse avalanche current ^a	L = 0.1 mH	I _{AS}	25	mJ
Single pulse avalanche energy ^a		E _{AS}	31.25	
Maximum power dissipation	T _C = 25 °C	P _D	65.2 ^b	W
	T _C = 125 °C		21.7 ^b	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	MAXIMUM	UNIT
Maximum junction-to-ambient (PCB mount) ^c		R _{thJA}	50	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	2.3	

Notes

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR4 material).
- Package limited.



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	250	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	150	μA
		$V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	5	mA
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8.3\text{ A}$	-	0.0372	0.0447	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 8.3\text{ A}$	-	11	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	560	-	pF
Output capacitance	C_{oss}		-	148	-	
Reverse transfer capacitance	C_{rss}		-	8	-	
Total gate charge	Q_g	$V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 8.3\text{ A}$	-	10.5	16	nC
Gate-source charge	Q_{gs}		-	2.7	-	
Gate-drain charge	Q_{gd}		-	3.1	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	1.44	7.2	14.4	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 75\text{ V}, R_L = 10.7\text{ }\Omega, I_D \cong 7\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	-	8	16	ns
Rise time	t_r		-	20	30	
Turn-off delay time	$t_{d(off)}$		-	15	25	
Fall time	t_f		-	30	50	
Drain-Source Body Diode Characteristics						
Pulse diode forward current ($t = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	42	A
Body diode voltage	V_{SD}	$I_F = 7\text{ A}, V_{GS} = 0\text{ V}$	-	0.85	1.5	V
Body diode reverse recovery time	t_{rr}	$I_F = 7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	68	102	ns
Body diode reverse recovery charge	Q_{rr}		-	0.21	0.32	μC
Reverse recovery fall time	t_a		-	56	-	ns
Reverse recovery rise time	t_b		-	12	-	
Body diode peak reverse recovery charge	$I_{RM(REC)}$		-	5.5	10	A

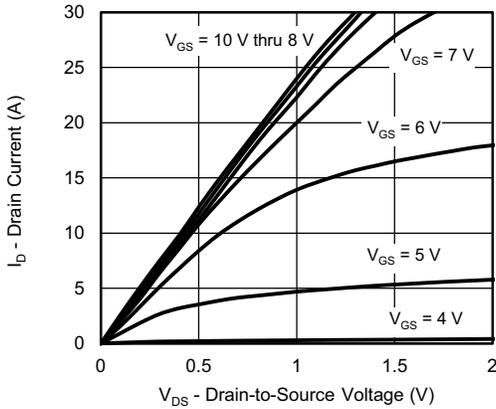
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

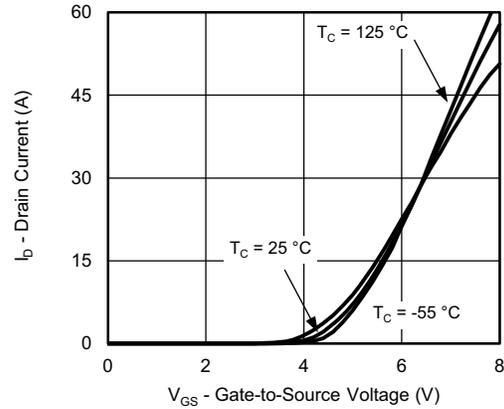
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



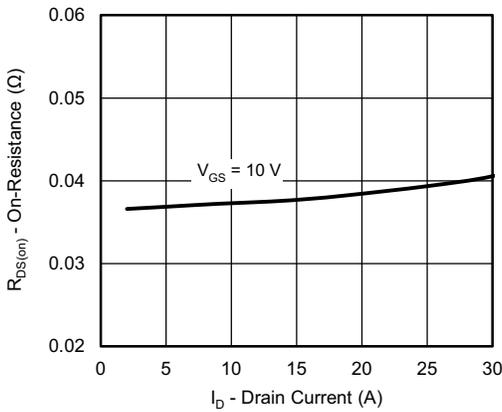
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



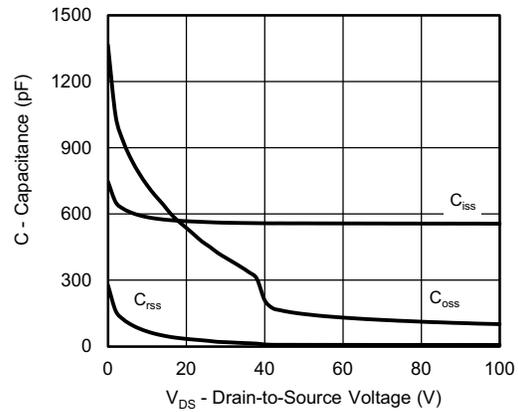
Output Characteristics



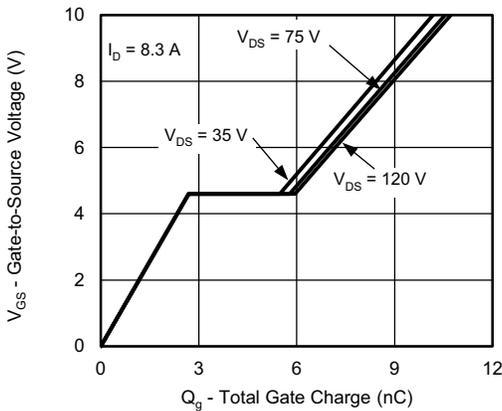
Transfer Characteristics



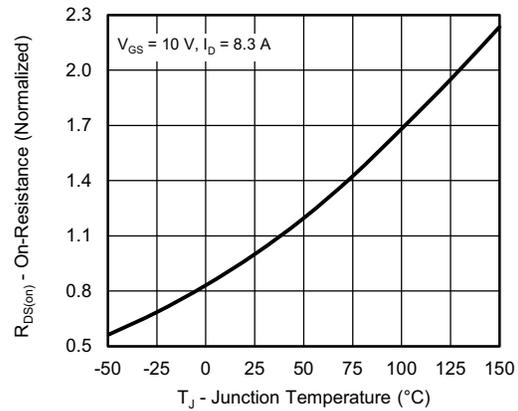
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

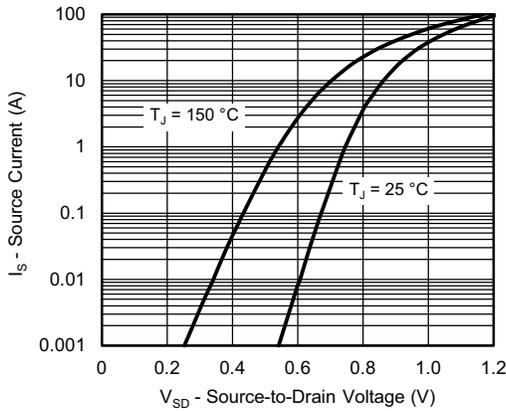


Gate Charge

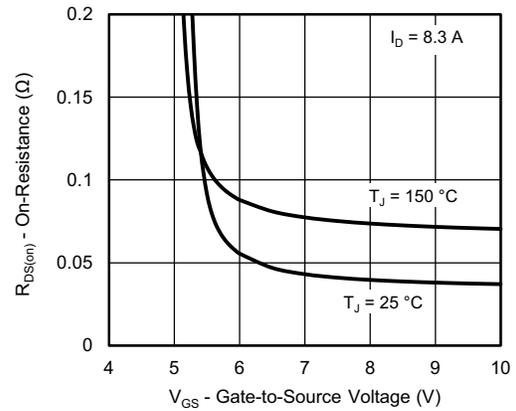


On-Resistance vs. Junction Temperature

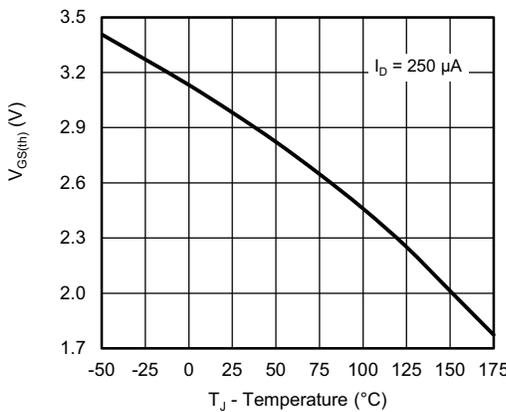
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



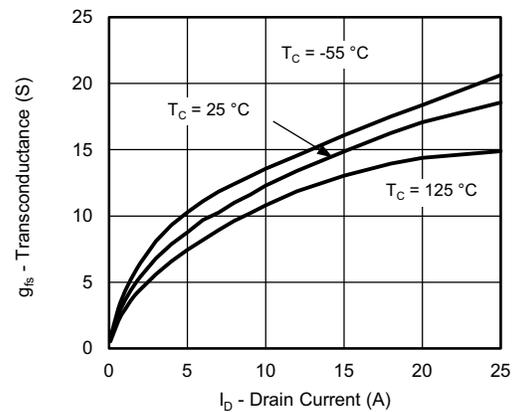
Source-Drain Diode Forward Voltage



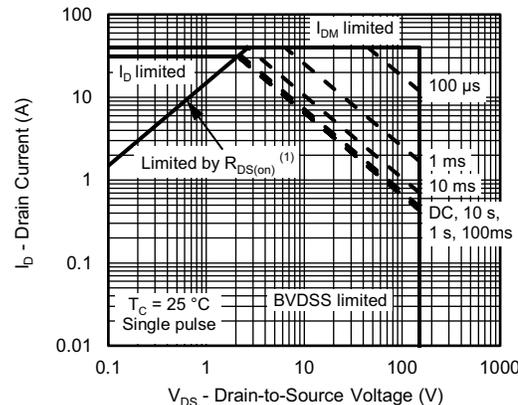
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Transconductance

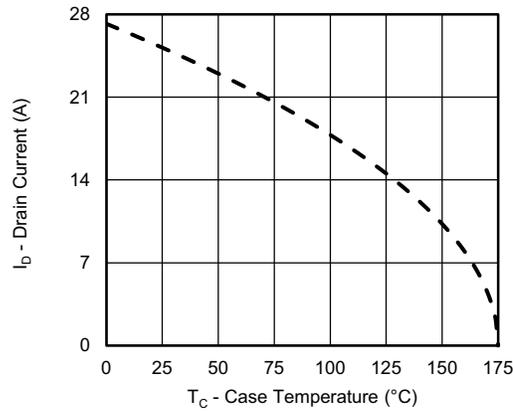


(1) $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

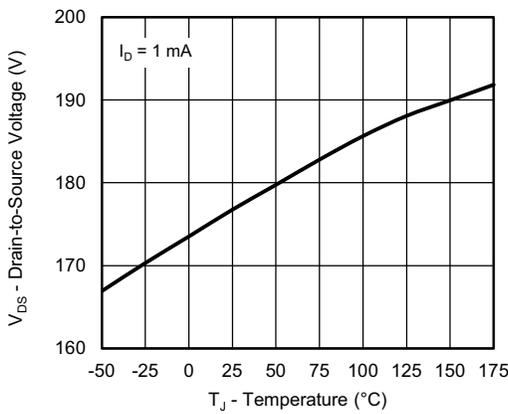
Safe Operating Area, Junction-to-Ambient



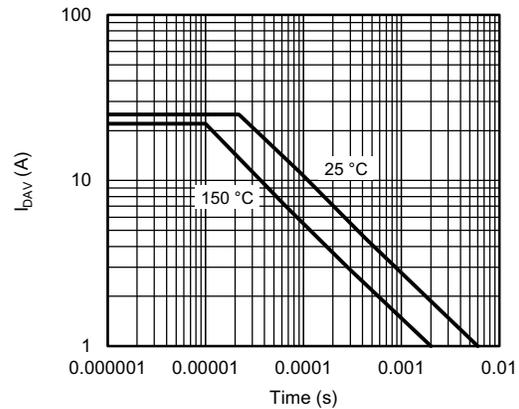
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Drain Source Breakdown vs. Junction Temperature



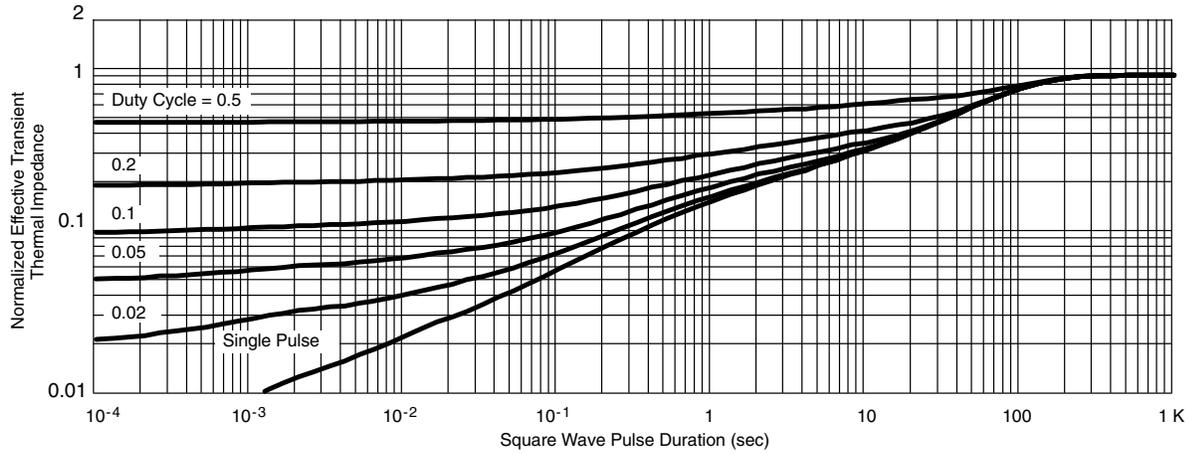
I_{DAV} vs. Time

Note

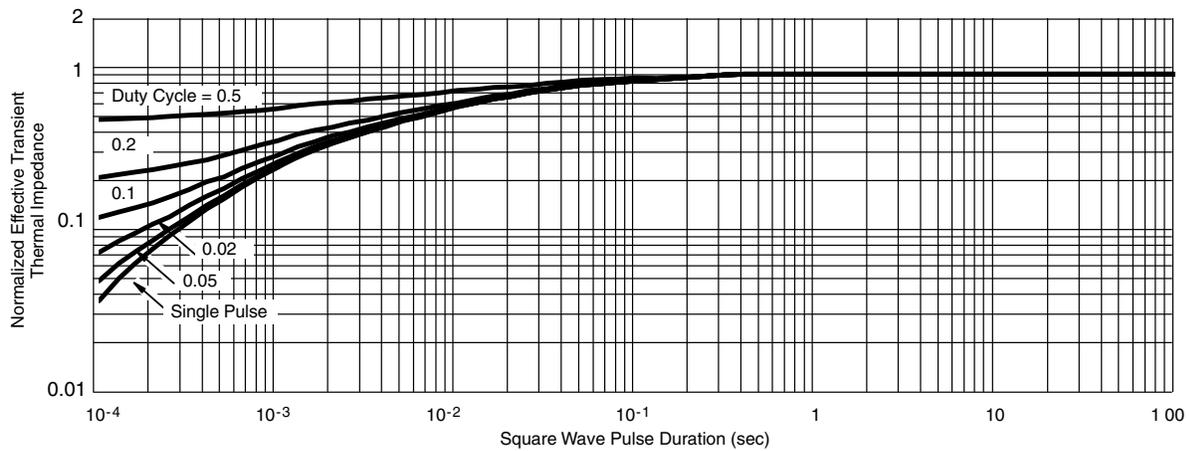
- a. The power dissipation P_D is based on $T_J \text{ max.} = 25 \text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



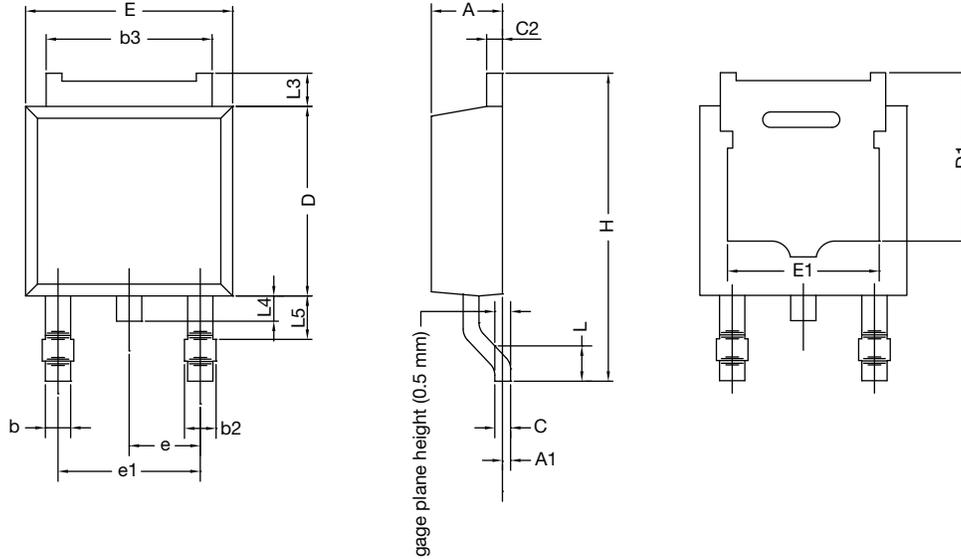
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76248.



TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



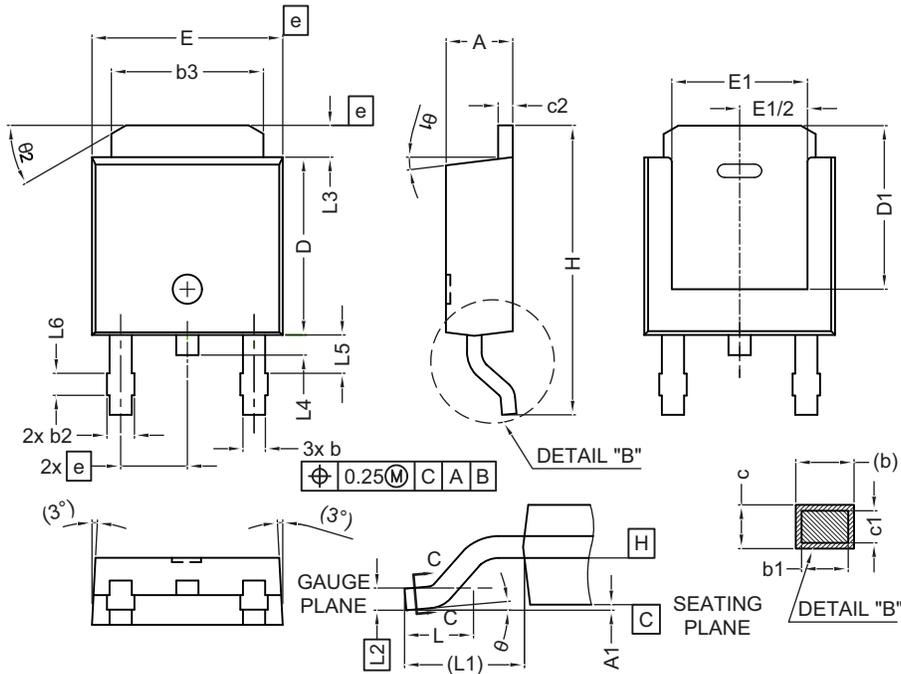
MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

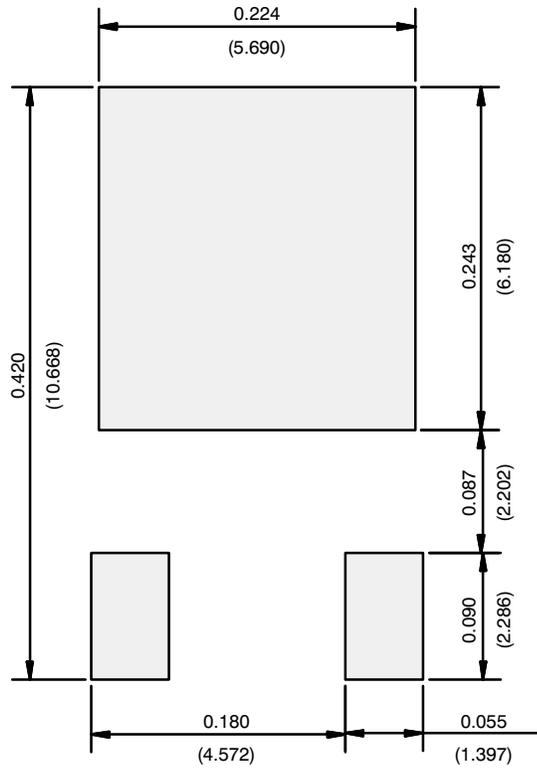
MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
 DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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