SPICE Device Model SQD40031EL



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Automotive P-Channel 30 V (D-S) 175 °C MOSFET

DESCRIPTION

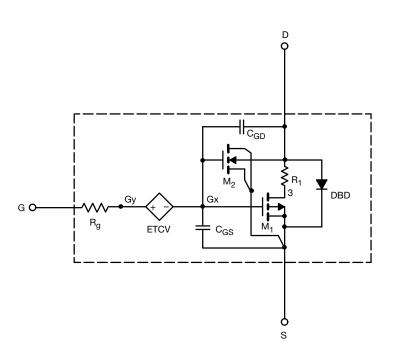
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	2	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = -10 \text{ V}, \text{ I}_{D} = -30 \text{ A}$	0.00264	0.00263	Ω
		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -25 \text{ A}$	0.00431	0.00425	
Forward transconductance ^a	9 _{fs}	$V_{DS} = -15 \text{ V}, \text{ I}_{D} = -30 \text{ A}$	114	98	S
Diode forward voltage	V _{SD}	I _S = -30 A	-0.79	-0.80	V
Dynamic ^b					
Input capacitance	C _{iss}	V _{DS} = -25 V, V _{GS} = 0 V, f = 1 MHz	11 500	11 085	pF
Output capacitance	Coss		1470	1342	
Reverse transfer capacitance	C _{rss}		1180	1181	
Total gate charge	Qg	V_{DS} = -15 V, V_{GS} = -10 V, I_D = -100 A	179	186	nC
Gate-source charge	Q _{gs}		37	28	
Gate-drain charge	Q _{gd}		40	28	

Notes

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

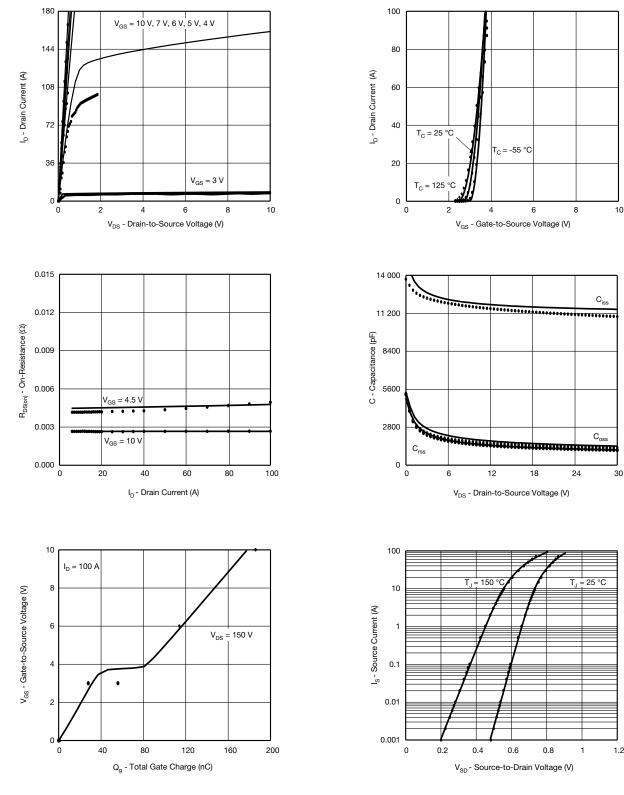
Document Number: 76322



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10

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

· Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.

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3

Document Number: 76322

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