

P-Channel 40 V (D-S) 175 °C MOSFET

DESCRIPTION

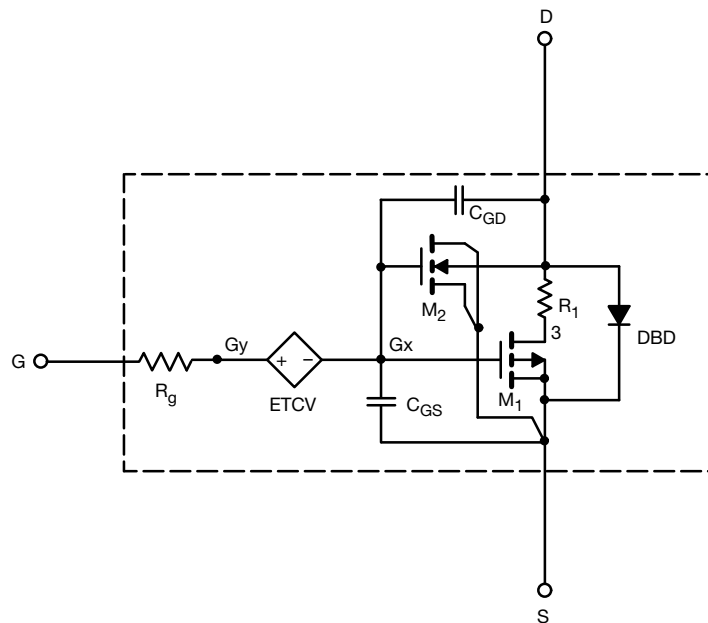
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



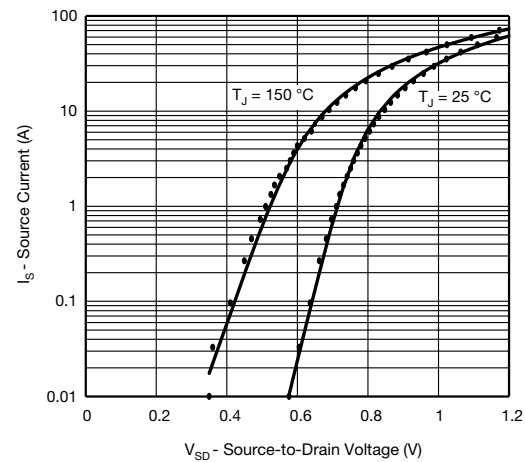
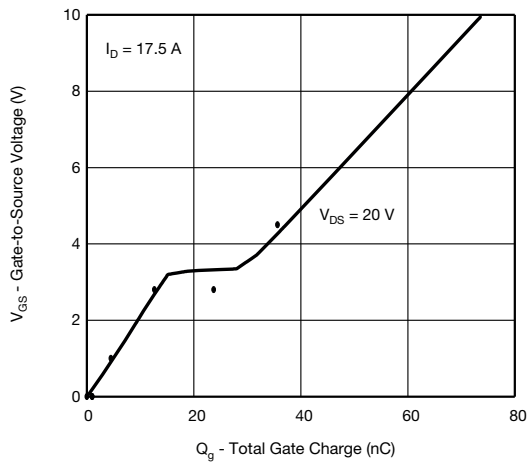
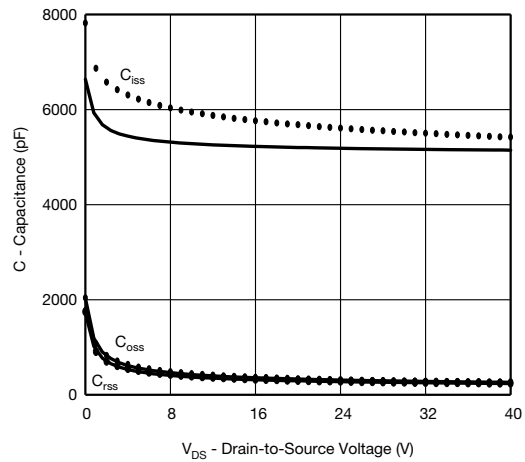
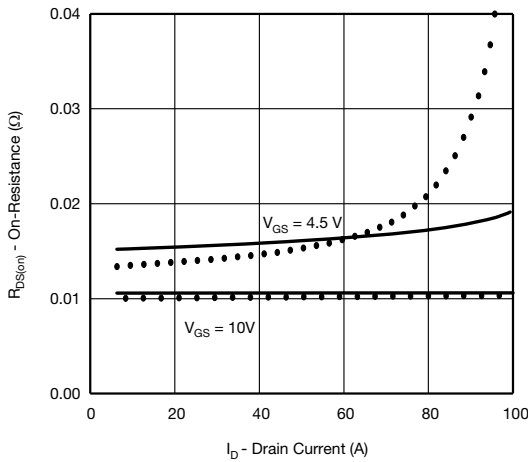
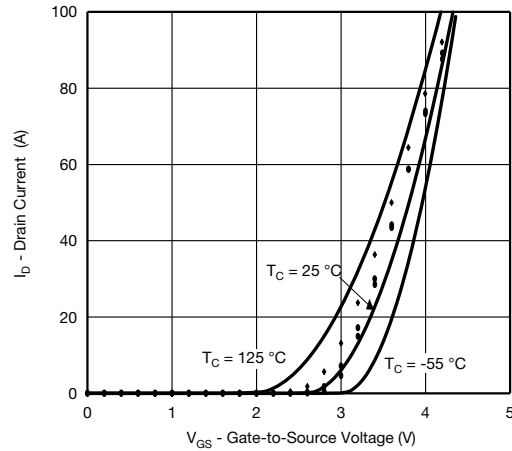
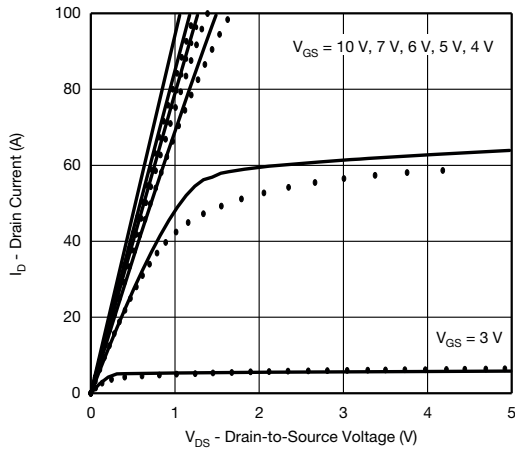
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|---|---------------------|--|----------------|---------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = -250 μA | 2 | - | V |
| Drain-source on-state resistance ^a | R _{DS(on)} | V _{GS} = -10 V, I _D = -17.5 A | 0.0105 | 0.0100 | Ω |
| | | V _{GS} = -4.5 V, I _D = -14.5 A | 0.0152 | 0.0135 | |
| Forward transconductance ^a | g _{fs} | V _{DS} = -10 V, I _D = -17.5 A | 38 | 13 | S |
| Diode forward voltage | V _{SD} | I _F = -14 A | -0.86 | -0.85 | V |
| Dynamic ^b | | | | | |
| Input capacitance | C _{iss} | V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz | 5200 | 5340 | pF |
| Output capacitance | C _{oss} | | 330 | 335 | |
| Reverse transfer capacitance | C _{rss} | | 294 | 303 | |
| Total gate charge | Q _g | V _{DS} = -20 V, V _{GS} = -10 V, I _D = -17.5 A | 74.3 | 74.3 | nC |
| Gate-source charge | Q _{gs} | | 14 | 12.7 | |
| Gate-drain charge | Q _{gd} | | 13 | 11.1 | |

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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