

Automotive N- and P-Channel 40 V (D-S) 175 °C MOSFET

DESCRIPTION

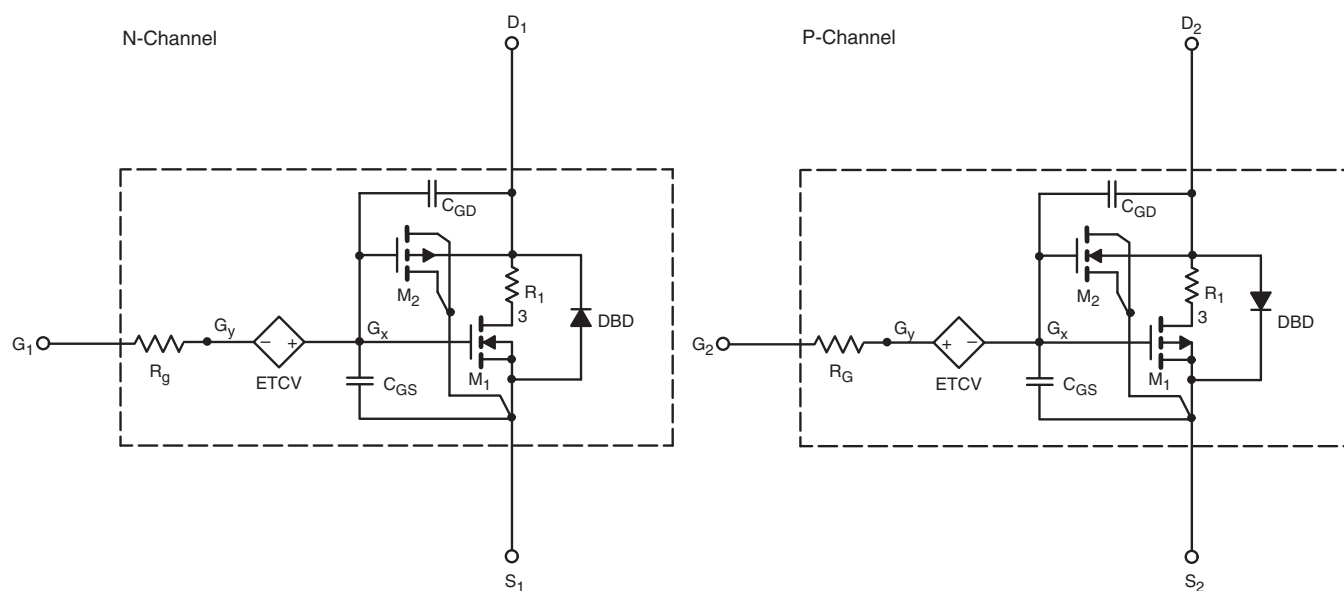
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and p-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



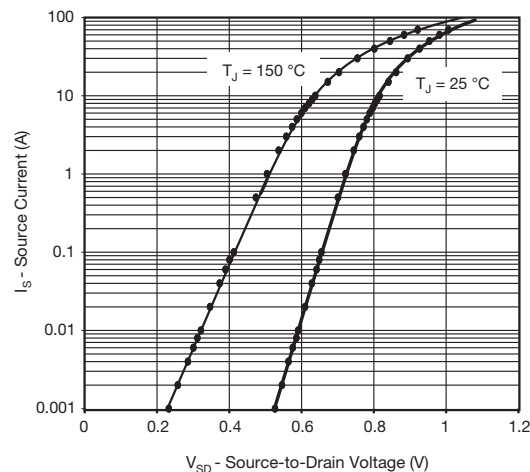
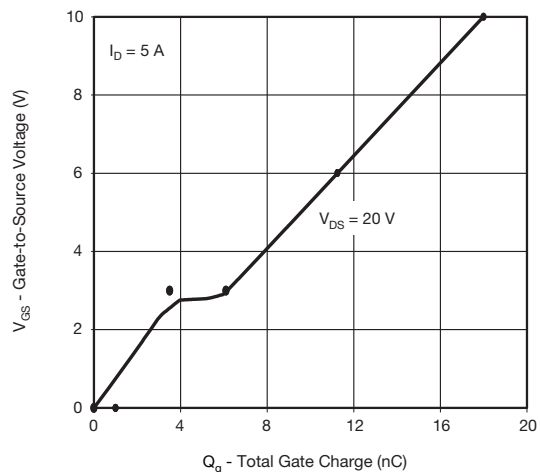
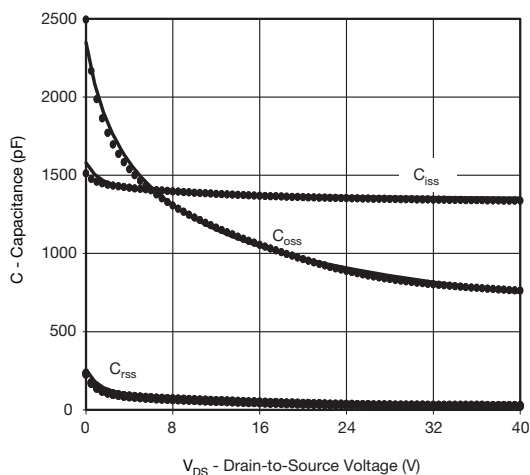
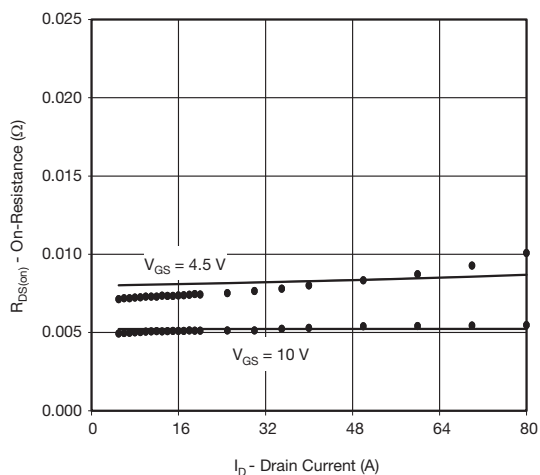
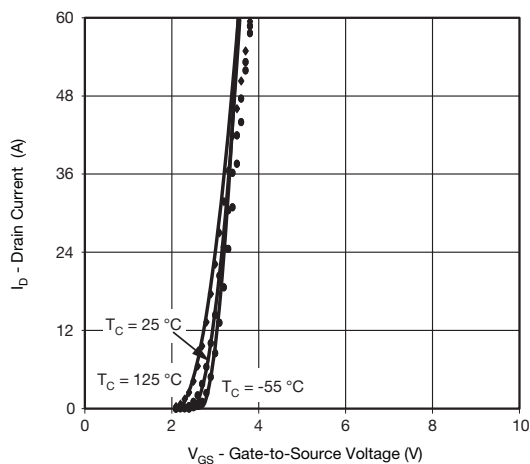
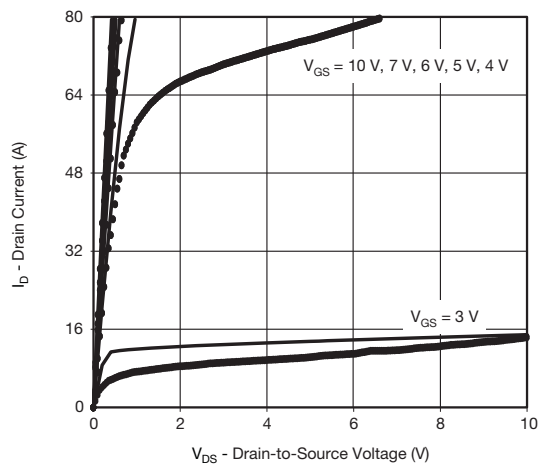
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		SIMULATED DATA	MEASURED DATA	UNIT
Static						
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	2	2	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	2	2	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 8 A	N-Ch	0.0052	0.0061	Ω
		V _{GS} = -10 V, I _D = -8 A	P-Ch	0.0114	0.0138	
		V _{GS} = 4.5 V, I _D = 5 A	N-Ch	0.0081	0.0088	
		V _{GS} = -4.5 V, I _D = -5 A	P-Ch	0.0173	0.0186	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 8 A	N-Ch	32	35	S
		V _{DS} = -15 V, I _D = -8 A	P-Ch	31	30	
Diode forward voltage ^a	V _{SD}	I _S = 8 A	N-Ch	0.80	0.80	V
		I _S = -8 A	P-Ch	-0.78	-0.79	
Dynamic ^b						
Input capacitance	C _{iss}	N-channel V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz P-channel V _{DS} = -25 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	1370	1355	pF
Output capacitance	C _{oss}		P-Ch	3630	3340	
			N-Ch	968	875	
			P-Ch	249	230	
			Reverse transfer capacitance	C _{rss}	N-Ch	
P-Ch	234				216	
Total gate charge	Q _g	N-channel V _{DS} = 20 V, V _{GS} = 10 V, I _D = 5 A P-channel V _{DS} = -20 V, V _{GS} = -10 V, I _D = -5 A	N-Ch	18	18	nC
Gate-source charge	Q _{gs}		P-Ch	53	56	
			N-Ch	3.5	3.5	
			P-Ch	8.5	8.5	
			Gate-drain charge	Q _{gd}	N-Ch	
P-Ch	9.9				9.9	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing



N-CHANNEL - COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)

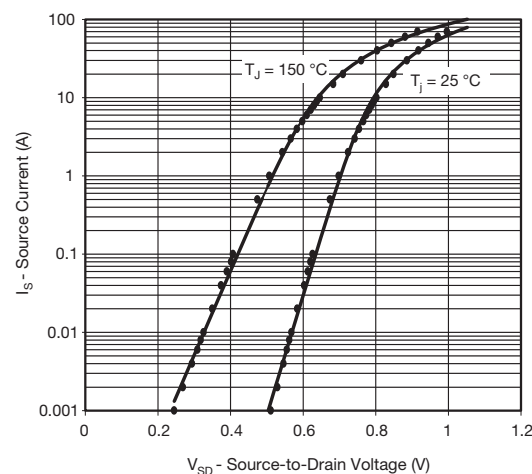
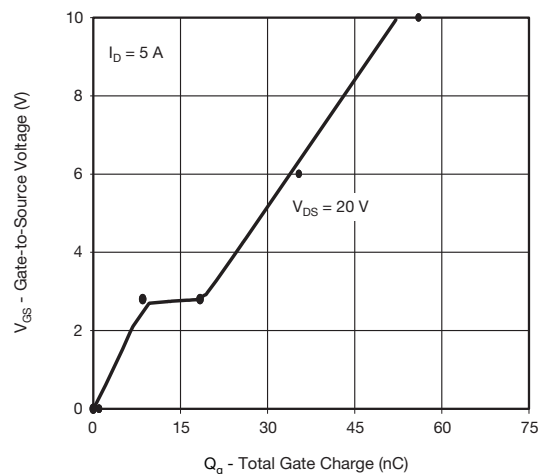
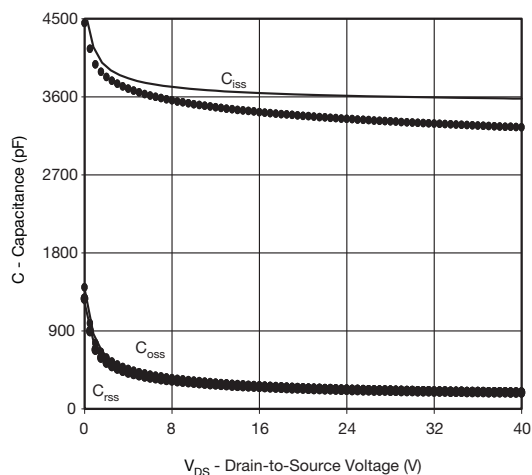
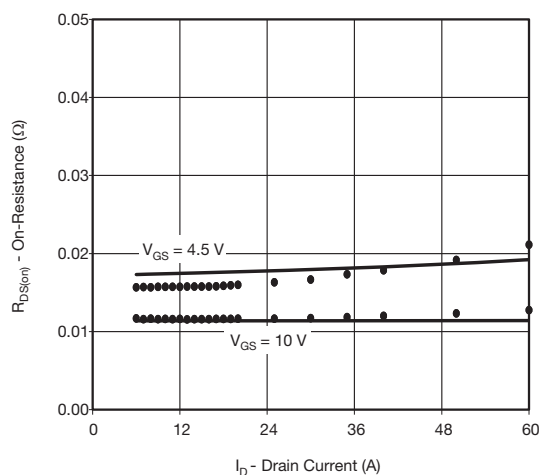
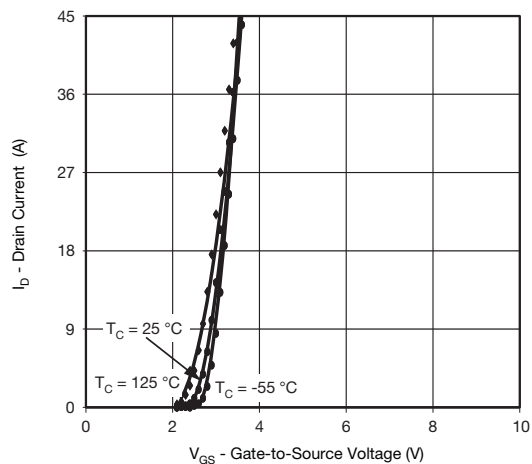
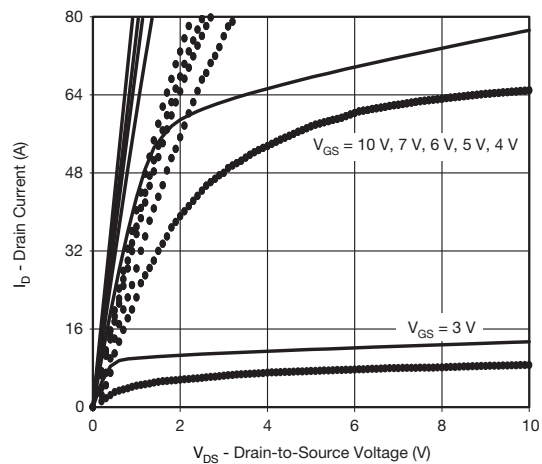


Note

- Dots and squares represent measured data



P-CHANNEL - COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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