Automotive Dual N-Channel 60 V (D-S) 175 °C MOSFET

DESCRIPTION

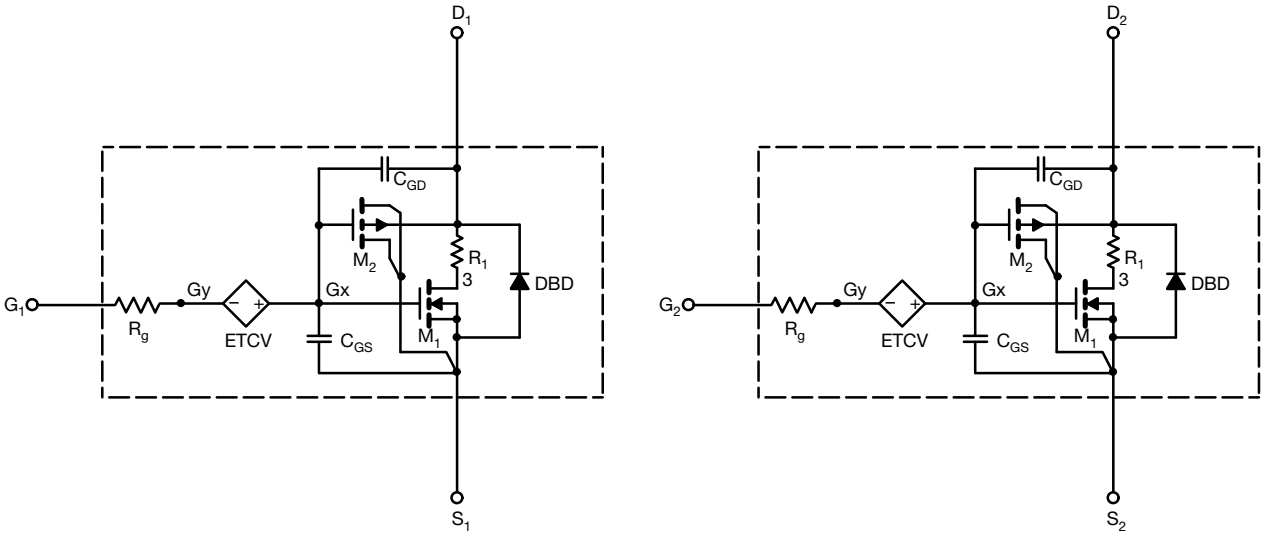
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	Ch-1	2	2	V
		V_{DS} = V_{GS}, I_D = -250 µA	Ch-2	2	2	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2 A	Ch-1	0.0293	0.0295	Ω
		V_{GS} = 10 V, I_D = 5 A	Ch-2	0.0123	0.0126	
		V_{GS} = 4.5 V, I_D = 1 A	Ch-1	0.0410	0.0400	
		V_{GS} = 4.5 V, I_D = 3 A	Ch-2	0.0169	0.0165	
Diode Forward Voltage [b]	V_{SD}	I_S = 2 A	Ch-1	0.79	0.81	V
		I_S = 5 A	Ch-2	0.79	0.80	
Dynamic [b]						
Input Capacitance	C_{iss}	N1-Channel V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz N2-Channel V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	456	410	pF
			Ch-2	1060	967	
Output Capacitance	C_{oss}		Ch-1	215	212	
			Ch-2	440	436	
Reverse Transfer Capacitance	C_{rss}		Ch-1	21	15	
			Ch-2	23	18	
Total Gate Charge	Q_g	N1-Channel V_{DS} = 30 V, V_{GS} = 10 V, I_D = 1 A N2-Channel V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A	Ch-1	6	6.5	nC
			Ch-2	13.4	14.5	
Gate-Source Charge	Q_{gs}		Ch-1	1.3	1.4	
			Ch-2	2.7	2.7	
Gate-Drain Charge	Q_{gd}		Ch-1	0.8	0.9	
			Ch-2	1.4	2.1	

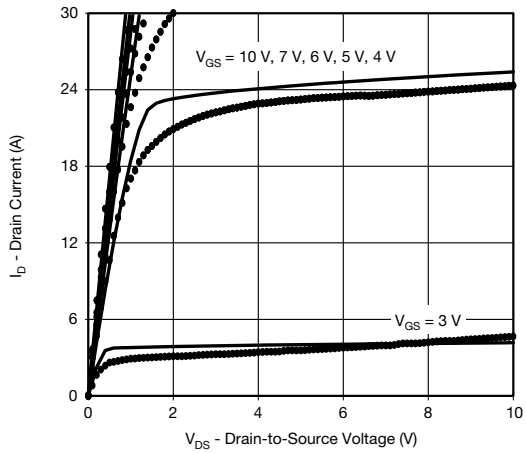
Notes

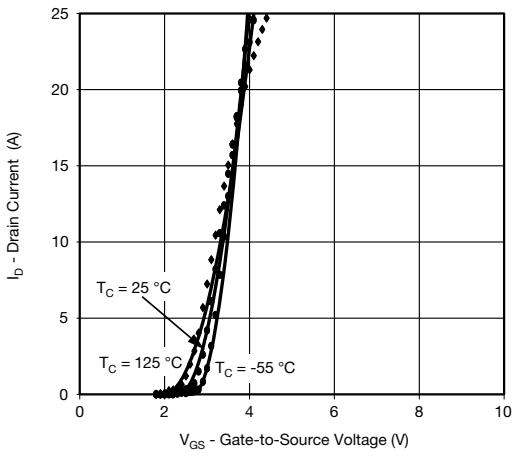
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

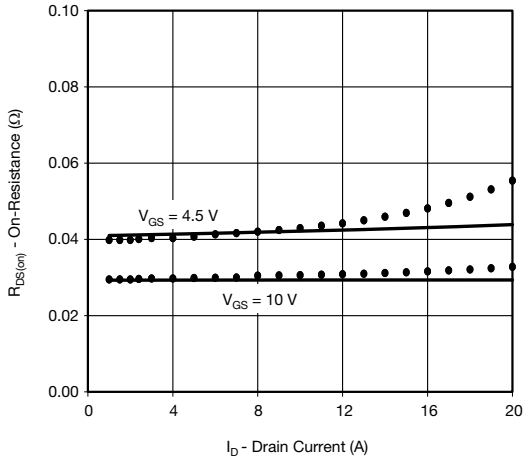
b. Guaranteed by design, not subject to production testing

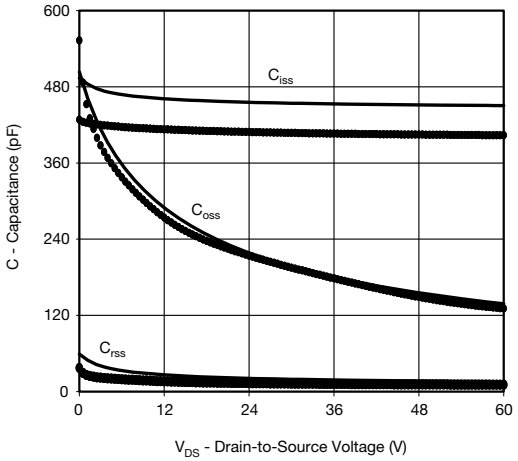
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

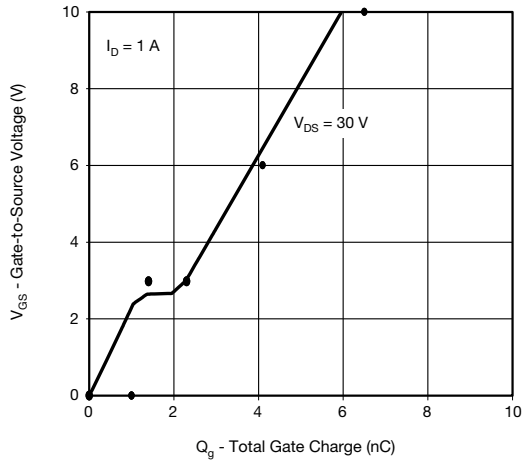
N1-Channel MOSFET

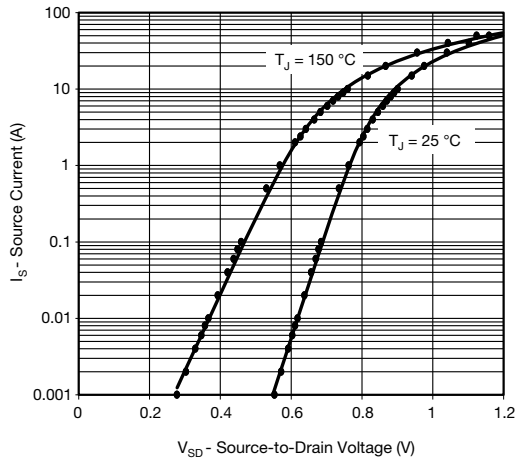










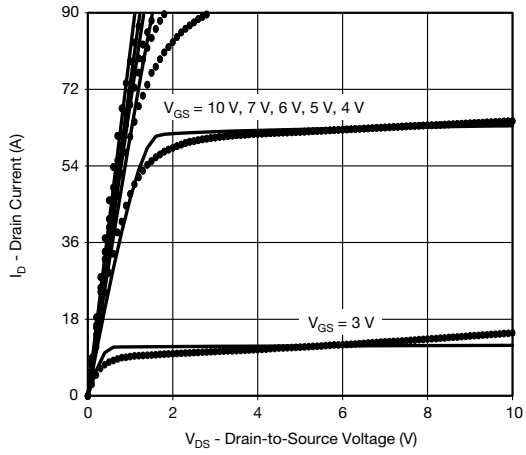


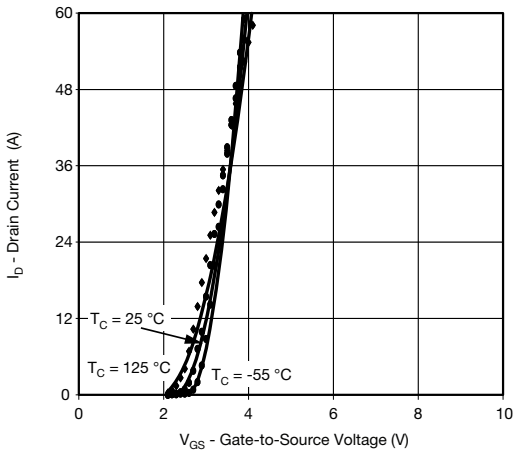
Note

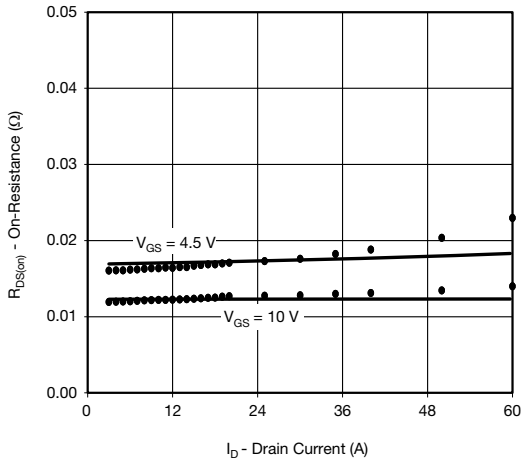
- Dots and squares represent measured data.

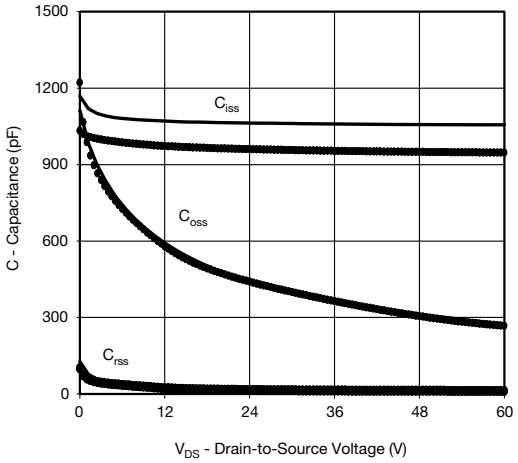
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

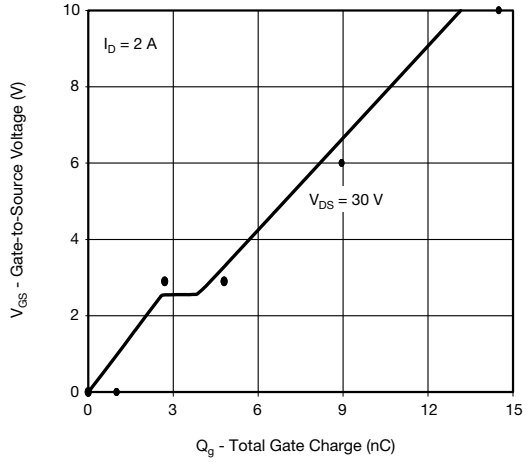
N2-Channel MOSFET

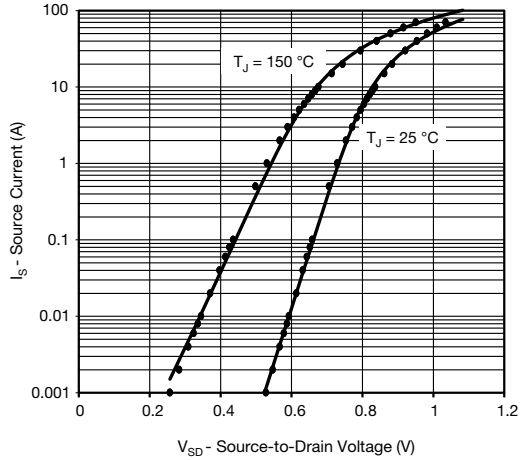












Note

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