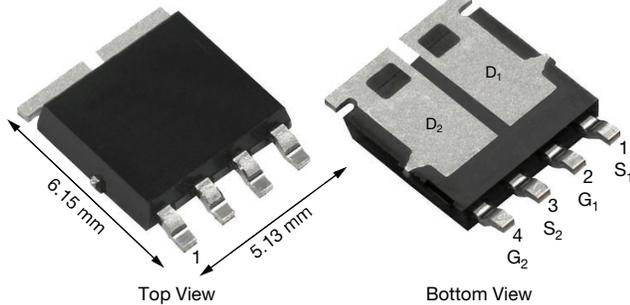
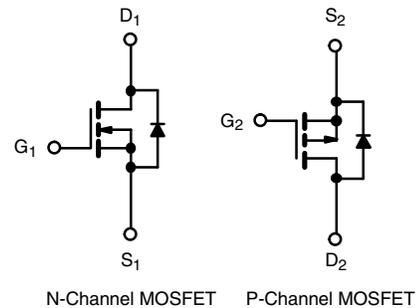


Automotive N- and P-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Dual

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_G and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V _{DS} (V)	100	-100
R _{DS(on)} (Ω) at V _{GS} = ± 10 V	0.0450	0.1460
R _{DS(on)} (Ω) at V _{GS} = ± 4.5 V	0.0580	0.2065
I _D (A)	15	-9.5
Configuration	N- and p-pair	

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ570EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage	V _{DS}	100	-100	V
Gate-source voltage	V _{GS}	± 20		
Continuous drain current	I _D	T _C = 25 °C	15 ^a	A
		T _C = 125 °C	9.6	
Continuous source current (diode conduction) ^a	I _S	15	-15	A
Pulsed drain current ^b	I _{DM}	40	-21	
Single pulse avalanche current	I _{AS}	L = 0.1 mH	13	-6
Single pulse avalanche Energy			E _{AS}	
Maximum power dissipation ^b	P _D	T _C = 25 °C	27	W
		T _C = 125 °C	9	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175		°C
Soldering recommendations (peak temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-ambient	R _{thJA}	85	85	°C/W
Junction-to-case (drain)	R _{thJC}	5.5	5.5	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT	
Static									
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch	100	-	-	V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		P-Ch	-100	-	-		
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch	1.5	2	2.5	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		P-Ch	-1.5	-2	-2.5		
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		N-Ch	-	-	± 100	nA	
				P-Ch	-	-	± 100		
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}$	N-Ch	-	-	1	μA	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -100\text{ V}$	P-Ch	-	-	-1		
		$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch	-	-	50		
		$V_{GS} = 0\text{ V}$	$V_{DS} = -100\text{ V}, T_J = 125\text{ }^\circ\text{C}$	P-Ch	-	-	-50		
		$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch	-	-	150		
		$V_{GS} = 0\text{ V}$	$V_{DS} = -100\text{ V}, T_J = 175\text{ }^\circ\text{C}$	P-Ch	-	-	-150		
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch	10	-	-	A	
		$V_{GS} = -10\text{ V}$	$V_{DS} \leq 5\text{ V}$	P-Ch	-6	-	-		
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 6\text{ A}$	N-Ch	-	0.0365	0.0450	Ω	
		$V_{GS} = -10\text{ V}$	$I_D = -6\text{ A}$	P-Ch	-	0.1184	0.1460		
		$V_{GS} = 10\text{ V}$	$I_D = 6\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch	-	-	0.0774		
		$V_{GS} = -10\text{ V}$	$I_D = -6\text{ A}, T_J = 125\text{ }^\circ\text{C}$	P-Ch	-	-	0.2435		
		$V_{GS} = 10\text{ V}$	$I_D = 6\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch	-	-	0.0978		
		$V_{GS} = -10\text{ V}$	$I_D = -6\text{ A}, T_J = 175\text{ }^\circ\text{C}$	P-Ch	-	-	0.2994		
		$V_{GS} = 4.5\text{ V}$	$I_D = 4\text{ A}$	N-Ch	-	0.0468	0.0580		
		$V_{GS} = -4.5\text{ V}$	$I_D = -4\text{ A}$	P-Ch	-	0.1669	0.2065		
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 6\text{ A}$		N-Ch	-	15	-	S	
		$V_{DS} = -15\text{ V}, I_D = -6\text{ A}$		P-Ch	-	7	-		
Dynamic ^b									
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	N-Ch	-	420	600	μF	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -25\text{ V}, f = 1\text{ MHz}$	P-Ch	-	480	650		
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	N-Ch	-	260	350	μF	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -25\text{ V}, f = 1\text{ MHz}$	P-Ch	-	250	350		
Reverse transfer capacitance	C_{rss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	N-Ch	-	17	25	μF	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -25\text{ V}, f = 1\text{ MHz}$	P-Ch	-	20	30		
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 50\text{ V}, I_D = 1\text{ A}$	N-Ch	-	9	15	nC	
		$V_{GS} = -10\text{ V}$	$V_{DS} = -50\text{ V}, I_D = -1\text{ A}$	P-Ch	-	12	20		
Gate-source charge ^c	Q_{gs}	$V_{GS} = 10\text{ V}$	$V_{DS} = 50\text{ V}, I_D = 1\text{ A}$	N-Ch	-	1.2	-	nC	
		$V_{GS} = -10\text{ V}$	$V_{DS} = -50\text{ V}, I_D = -1\text{ A}$	P-Ch	-	2	-		
Gate-drain charge ^c	Q_{gd}	$V_{GS} = 10\text{ V}$	$V_{DS} = 50\text{ V}, I_D = 1\text{ A}$	N-Ch	-	1.9	-	nC	
		$V_{GS} = -10\text{ V}$	$V_{DS} = -50\text{ V}, I_D = -1\text{ A}$	P-Ch	-	3	-		
Gate resistance	R_g	$f = 1\text{ MHz}$			N-Ch	1.3	2.7	4.5	Ω
					P-Ch	5	10.2	15.5	



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 5\ \Omega$	N-Ch	-	8	15	ns
		$V_{DD} = -50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 5\ \Omega$	P-Ch	-	12	20	
Rise time ^c	t_r	$V_{DD} = 50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 5\ \Omega$	N-Ch	-	4	10	
		$V_{DD} = -50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 5\ \Omega$	P-Ch	-	5	10	
Turn-off delay time ^c	$t_{d(off)}$	$V_{DD} = 50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 5\ \Omega$	N-Ch	-	20	35	
		$V_{DD} = -50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 5\ \Omega$	P-Ch	-	30	50	
Fall time ^c	t_f	$V_{DD} = 50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 5\ \Omega$	N-Ch	-	17	30	
		$V_{DD} = -50\text{ V}$, $R_L = 50\ \Omega$, $I_D \cong -1\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 5\ \Omega$	P-Ch	-	15	25	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I_{SM}		N-Ch	-	-	40	A
			P-Ch	-	-	-21	
Forward voltage	V_{SD}	$I_S = 6\text{ A}$	N-Ch	-	0.89	1.2	V
		$I_S = -6\text{ A}$	P-Ch	-	-0.89	-1.2	

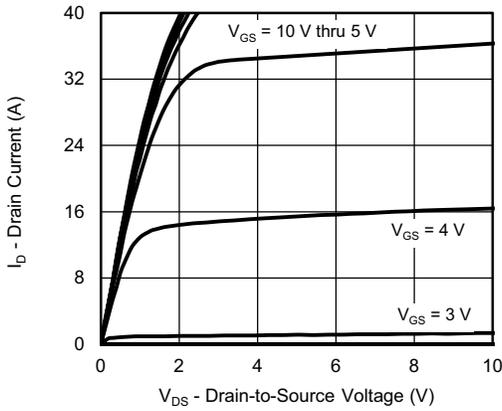
Notes

- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing
- Independent of operating temperature

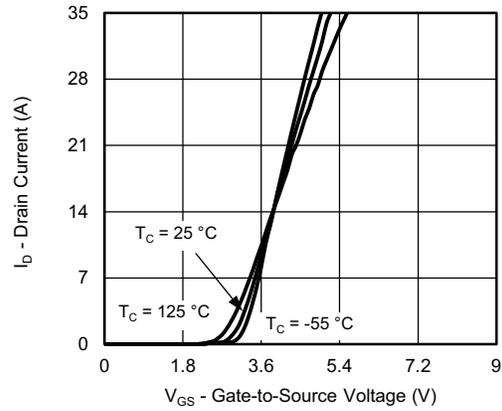
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



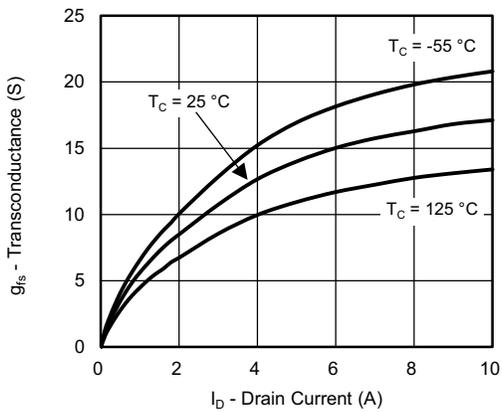
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



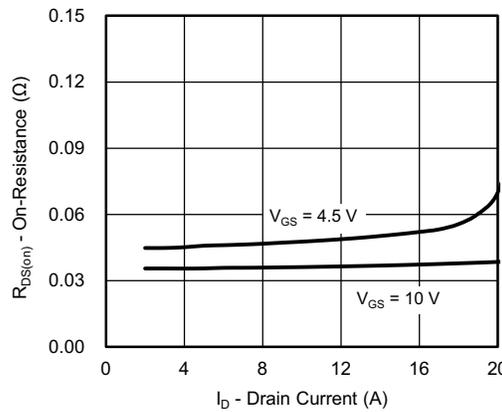
Output Characteristics



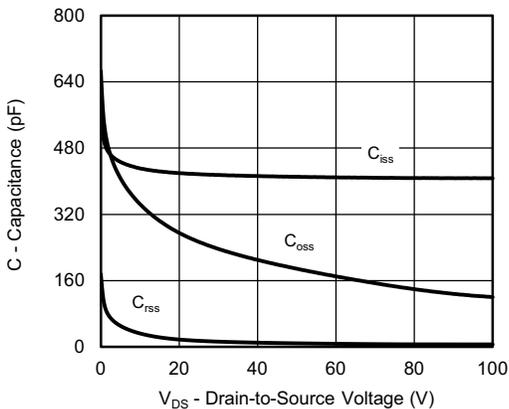
Transfer Characteristics



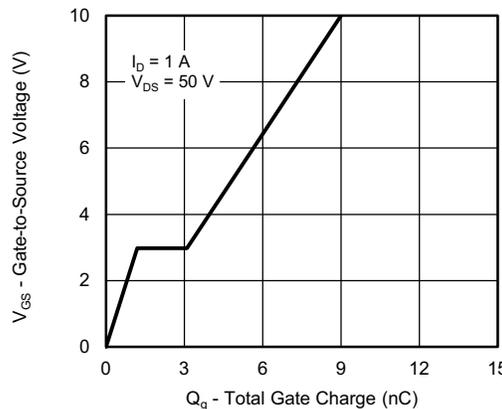
Transconductance



On-Resistance vs. Drain Current

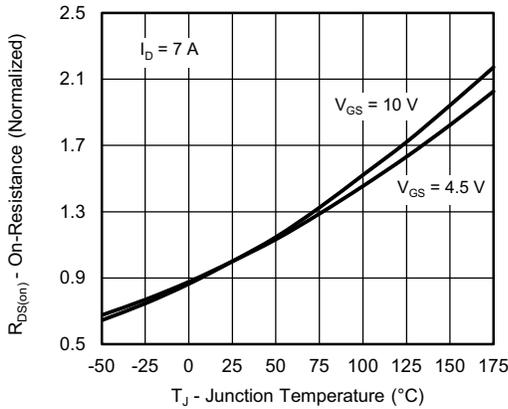


Capacitance

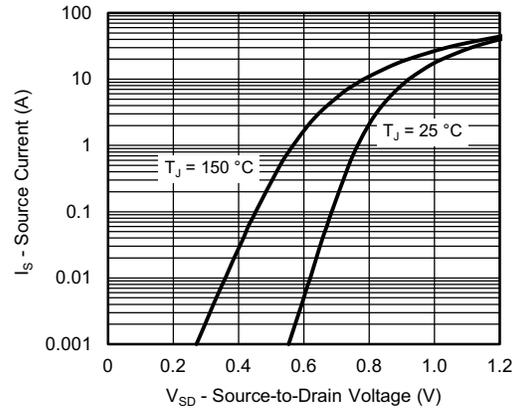


Gate Charge

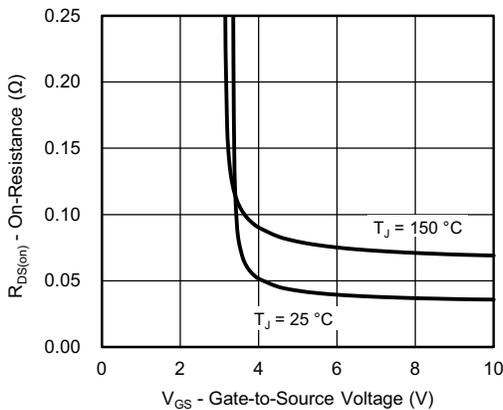
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



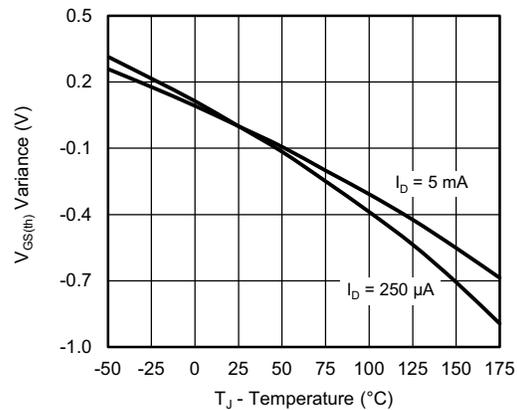
On-Resistance vs. Junction Temperature



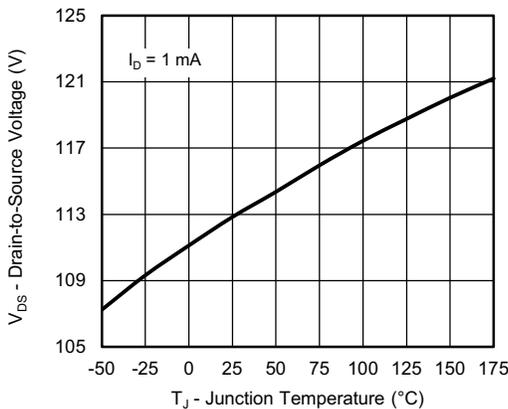
Source Drain Diode Forward Voltage



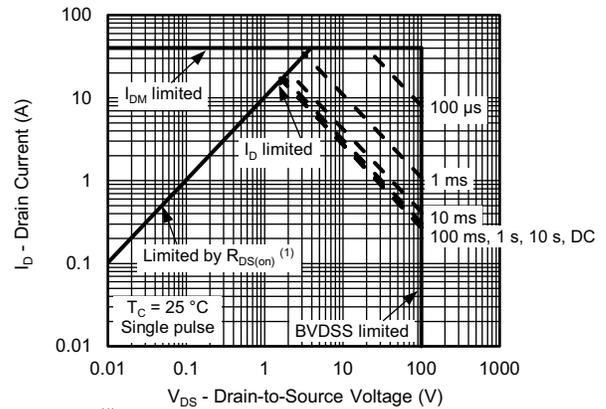
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



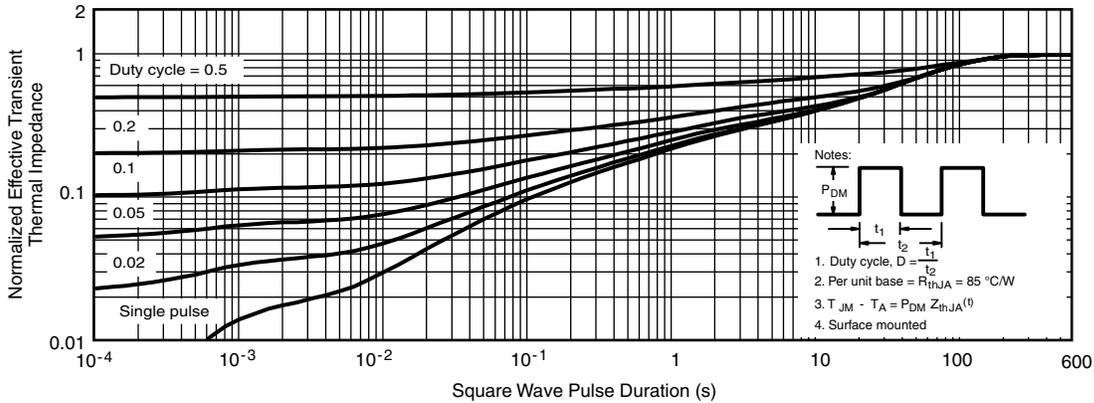
Drain Source Breakdown vs. Junction Temperature



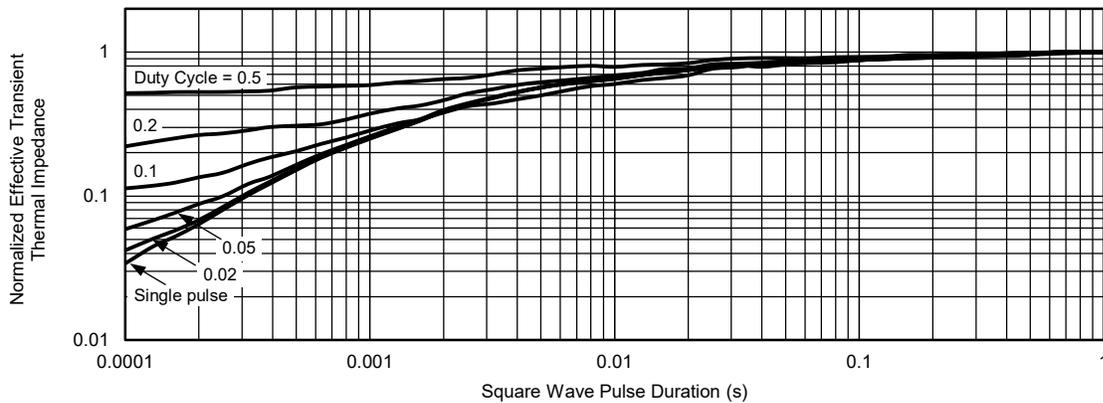
Safe Operating Area



N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

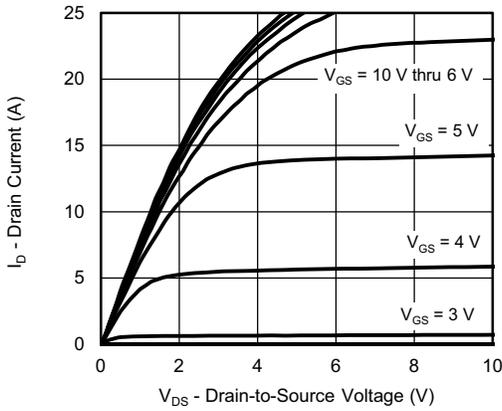


Normalized Thermal Transient Impedance, Junction-to-Case

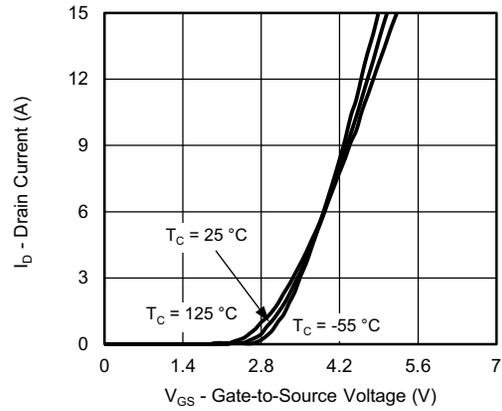
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

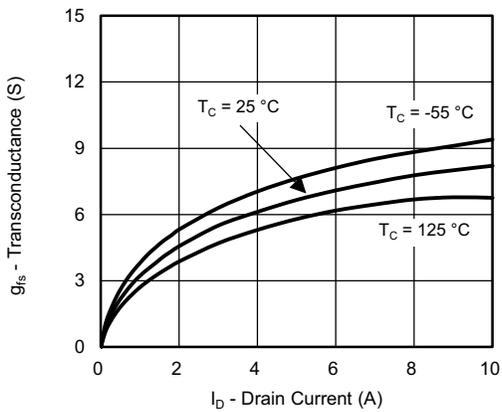
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



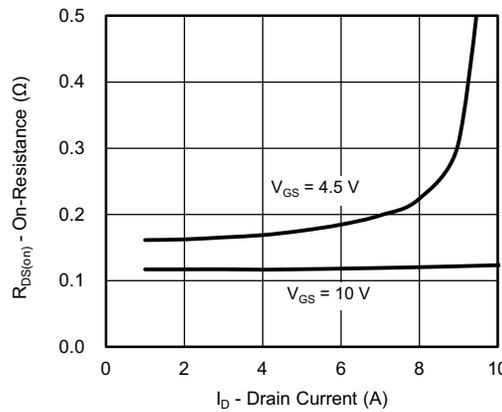
Output Characteristics



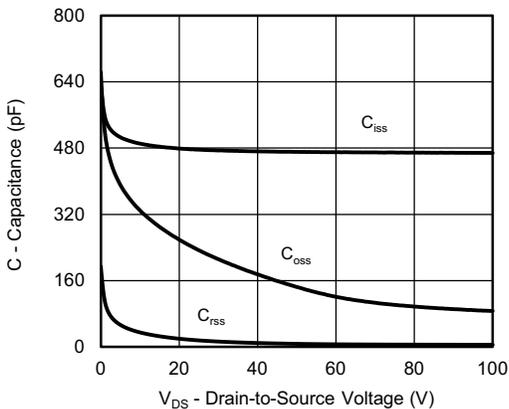
Transfer Characteristics



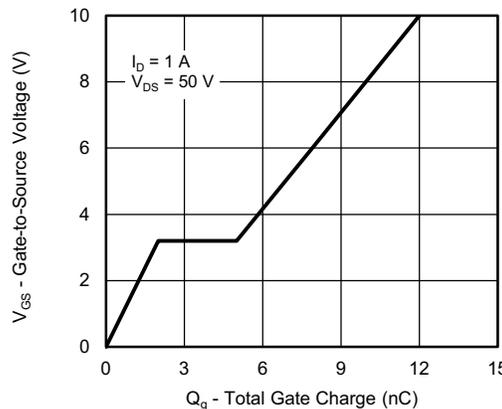
Transconductance



On-Resistance vs. Drain Current



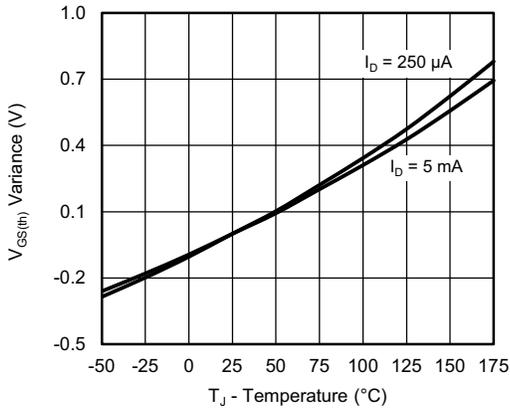
Capacitance



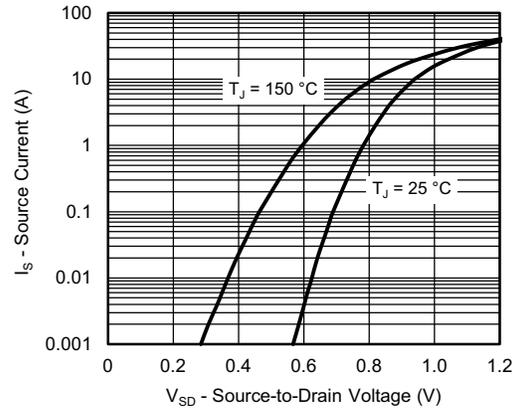
Gate Charge



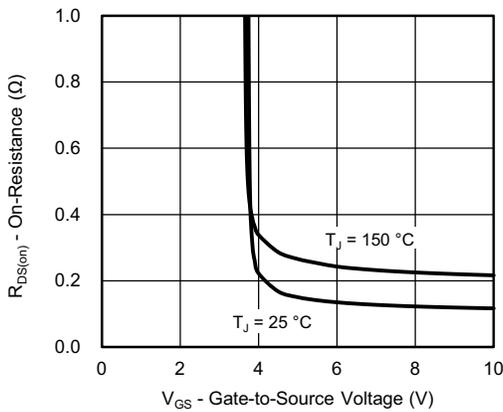
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



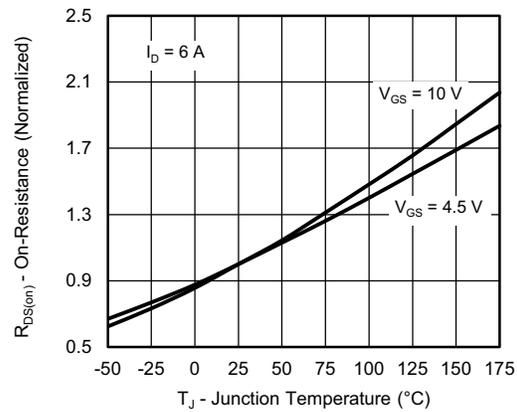
Threshold Voltage



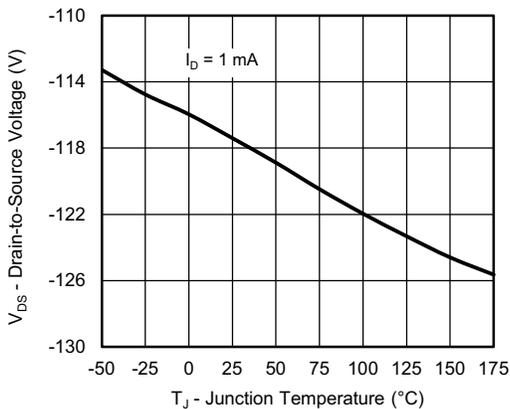
Source Drain Diode Forward Voltage



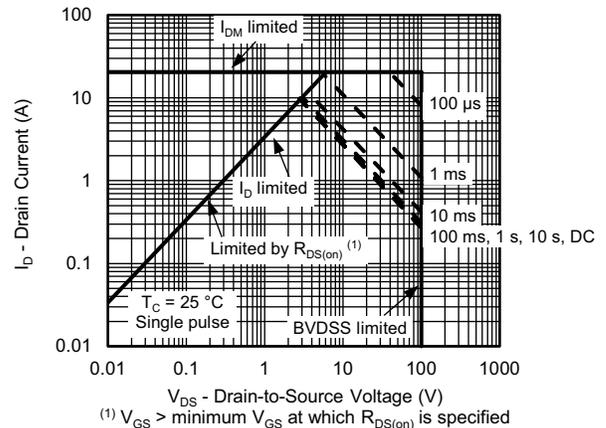
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature



Drain Source Breakdown vs. Junction Temperature

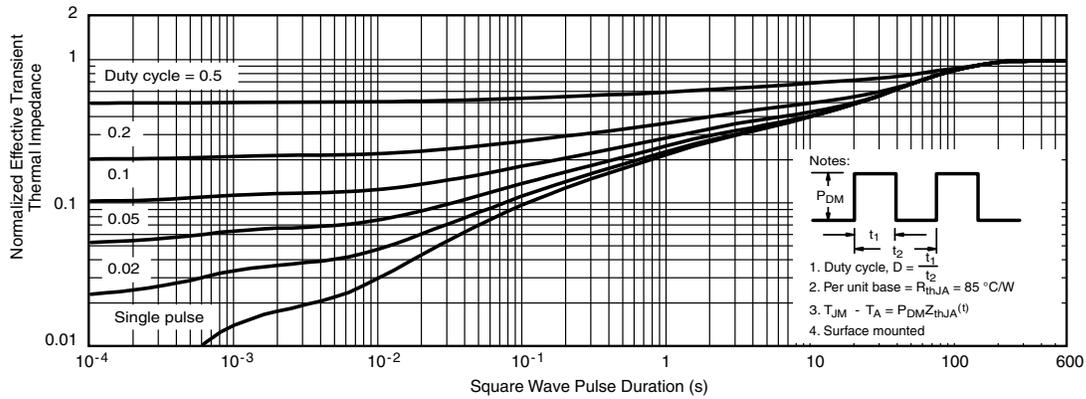


(1) $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

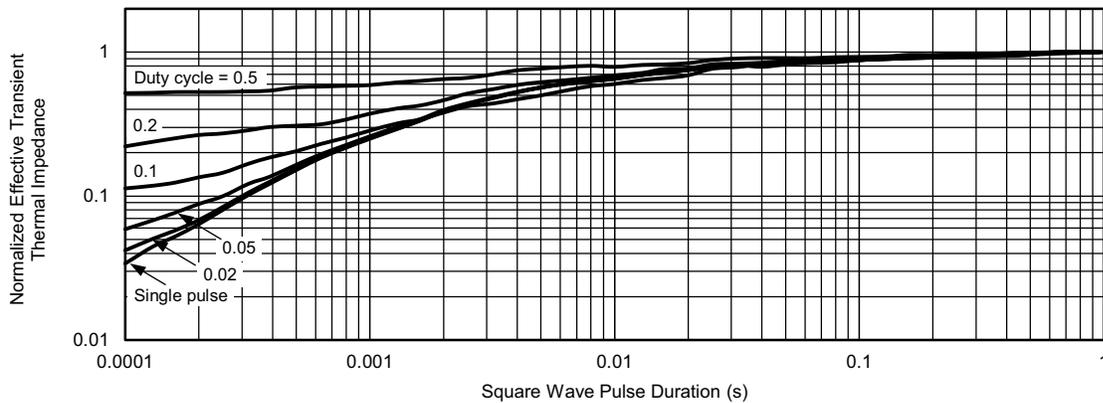
Safe Operating Area



P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

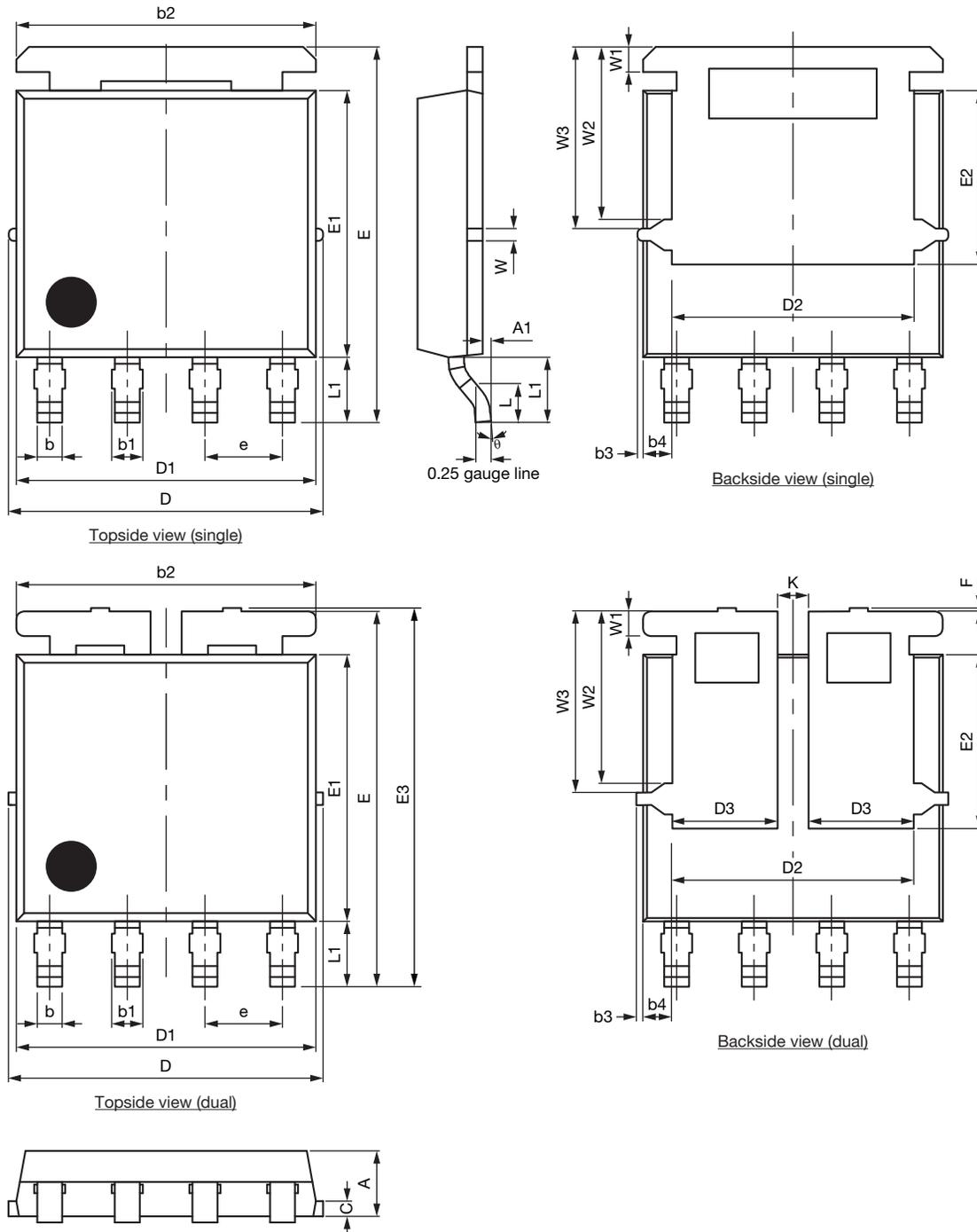
Note

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 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^\circ\text{C}$)
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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76453.



PowerPAK® SO-8L Case Outline 2





DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	6.05	6.22	6.40	0.238	0.245	0.252
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C23-1026-Rev. D, 25-Sep-2023 DWG: 6044						

Note

- Millimeters will govern



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