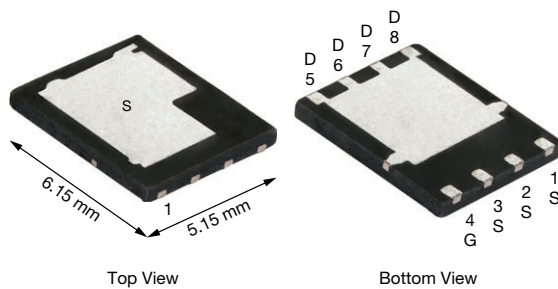


## N-Channel 45 V (D-S) MOSFET

**PowerPAK® SO-8DC**


Top View

Bottom View

PRODUCT SUMMARY	
$V_{DS}$ (V)	45
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.00120
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.00180
$Q_g$ typ. (nC)	50.5
$I_D$ (A) <sup>a</sup>	208
Configuration	Single

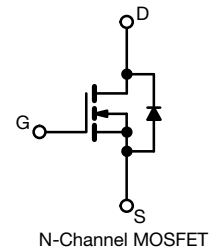
### FEATURES

- TrenchFET® Gen IV power MOSFET
- 45 V Drain-source break-down voltage
- Tuned for low  $Q_g$  and  $Q_{oss}$
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Motor drive control



ORDERING INFORMATION	
Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR608DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	45	V
Gate-source voltage	$V_{GS}$	+20, -16	
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	208
		$T_C = 70$ °C	166
		$T_A = 25$ °C	51 <sup>b, c</sup>
		$T_A = 70$ °C	40.8 <sup>b, c</sup>
Pulsed drain current ( $t = 100$ $\mu$ s)	$I_{DM}$	400	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	5.6 <sup>b, c</sup>
Single pulse avalanche current	$I_{AS}$	50	mJ
Single pulse avalanche Energy	$E_{AS}$	125	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	104
		$T_C = 70$ °C	66.6
		$T_A = 25$ °C	6.25 <sup>b, c</sup>
		$T_A = 70$ °C	4 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS								
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT				
Maximum junction-to-ambient <sup>b, f</sup>	$R_{thJA}$	15	20		°C/W			
Maximum junction-to-case (drain)						Steady state	0.9	1.2
Maximum junction-to-case (source)						Steady state	1.1	1.4

#### Notes

- Based on  $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W
- Package limited



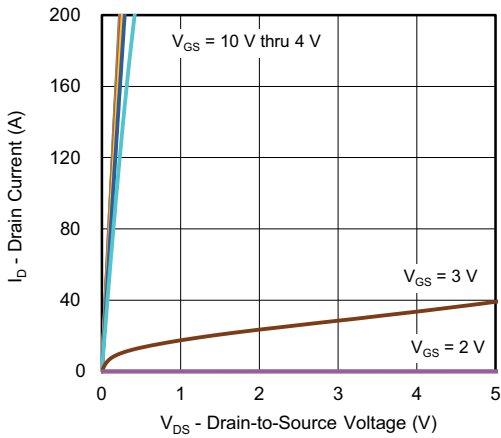
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	45	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	29	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-5.8	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.1	-	2.3	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = +20, -16\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 45\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 45\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$	50	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$	-	0.00100	0.00120	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 20\text{ A}$	-	0.00136	0.00180	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}$ , $I_D = 20\text{ A}$	-	120	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	-	8900	-	pF
Output capacitance	$C_{oss}$		-	1244	-	
Reverse transfer capacitance	$C_{rss}$		-	120	-	
$C_{rss}/C_{iss}$ ratio			-	0.0135	0.0270	
Total gate charge	$Q_g$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$	-	111	167	nC
Gate-source charge	$Q_{gs}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 20\text{ A}$	-	50.5	76	
Gate-drain charge	$Q_{gd}$		-	26	-	
Output charge	$Q_{oss}$		$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$	-	7.8	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.3	0.88	1.5	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$ , $R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	-	19	38	ns
Rise time	$t_r$		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	50	100	
Fall time	$t_f$		-	8	16	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$ , $R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\text{ }\Omega$	-	52	104	
Rise time	$t_r$		-	86	172	
Turn-off delay time	$t_{d(off)}$		-	50	100	
Fall time	$t_f$		-	25	50	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	94.5	A
Pulse diode forward current ( $t_p = 100\text{ }\mu\text{s}$ )	$I_{SM}$		-	-	400	
Body diode voltage	$V_{SD}$	$I_S = 10\text{ A}$	-	0.7	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	-	52	104	ns
Body diode reverse recovery charge	$Q_{rr}$		-	71	142	nC
Reverse recovery fall time	$t_a$		-	32	-	ns
Reverse recovery rise time	$t_b$		-	20	-	

**Notes**

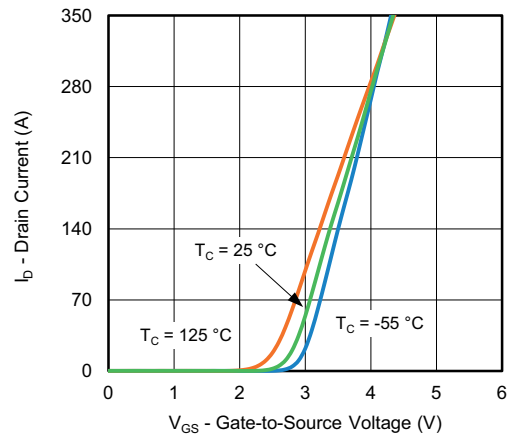
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

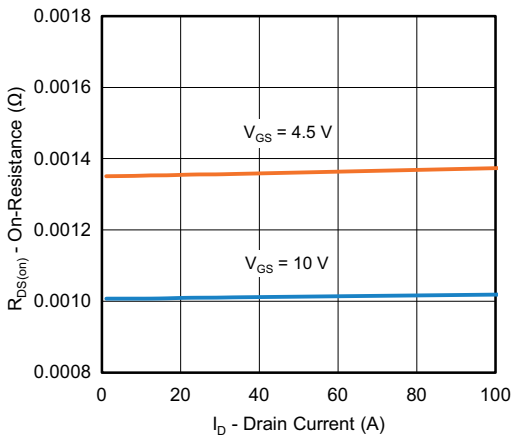
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



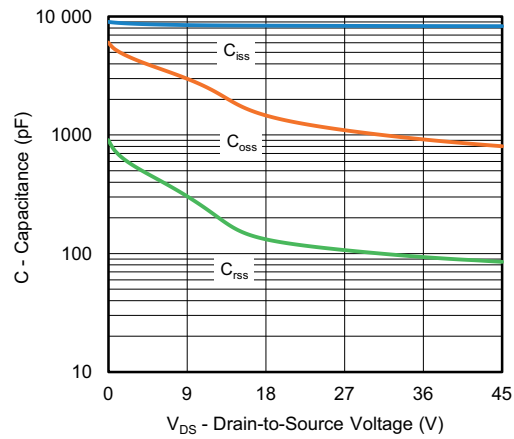
**Output Characteristics**



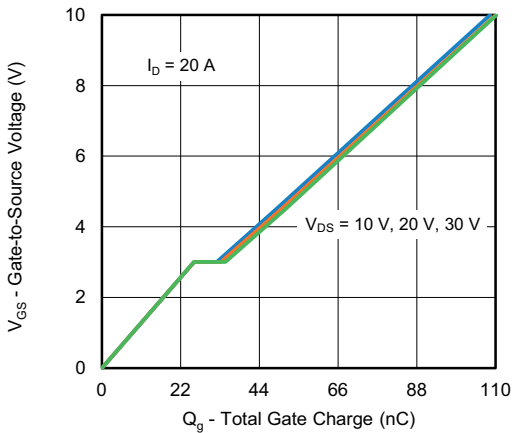
**Transfer Characteristics**



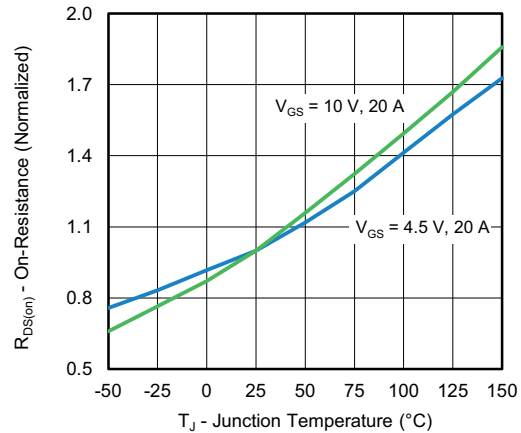
**On-Resistance vs. Drain Current**



**Capacitance**



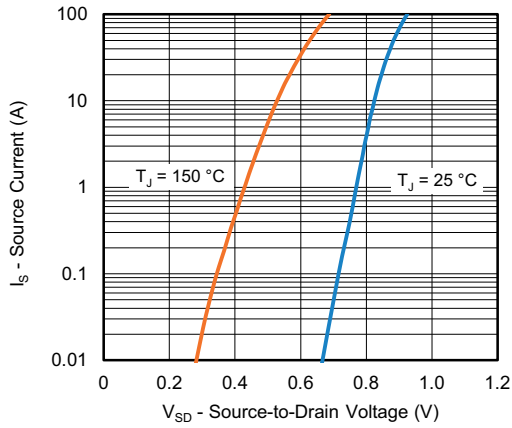
**Gate Charge**



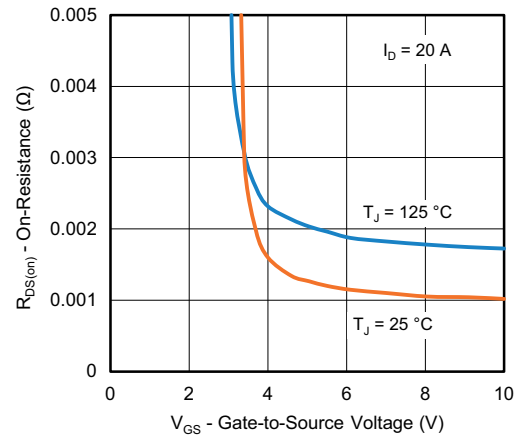
**On-Resistance vs. Junction Temperature**



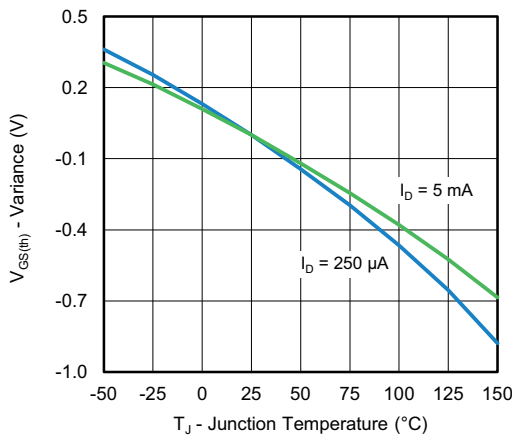
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



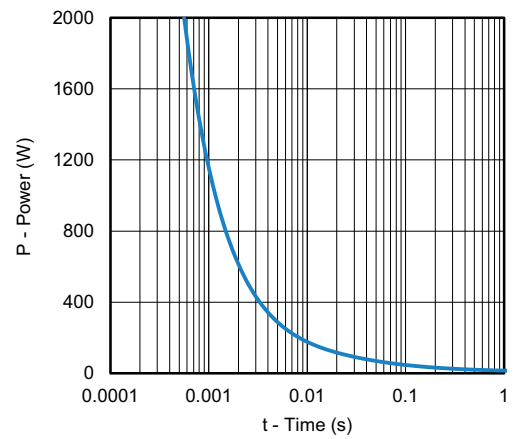
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



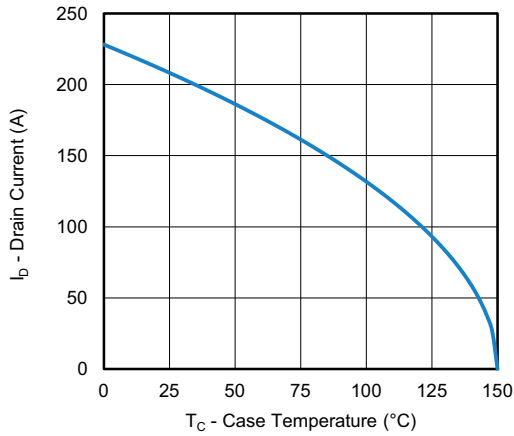
Threshold Voltage



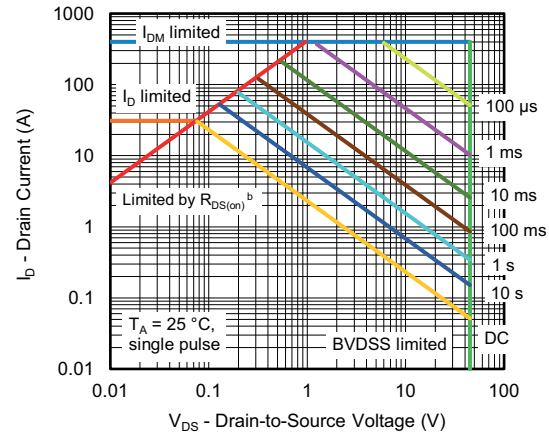
Single Pulse Power, Junction-to-Ambient



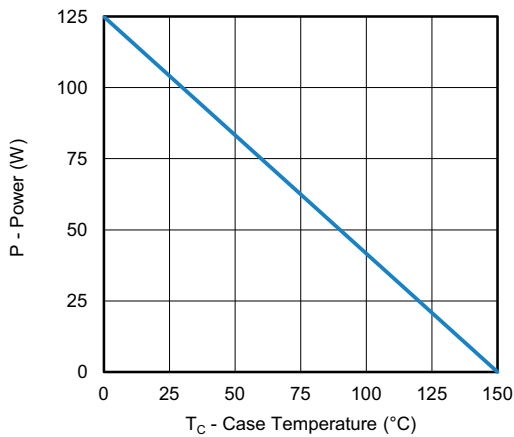
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



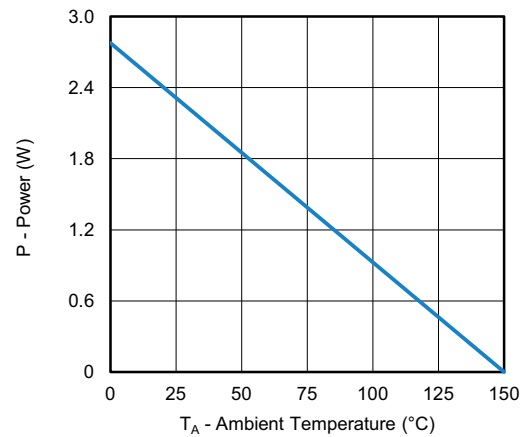
Current Derating <sup>a</sup>



Safe Operating Area



Power, Junction-to-Case



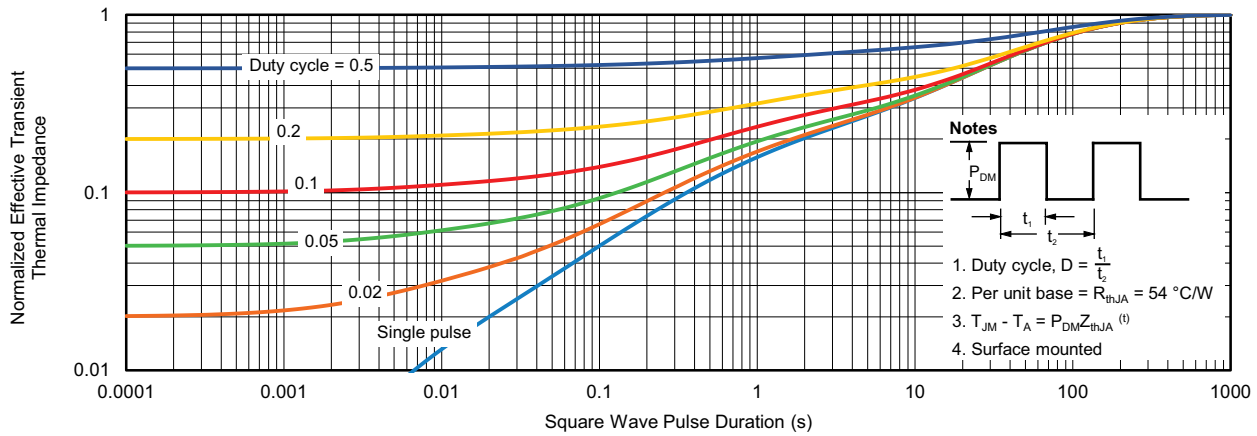
Power, Junction-to-Ambient

Notes

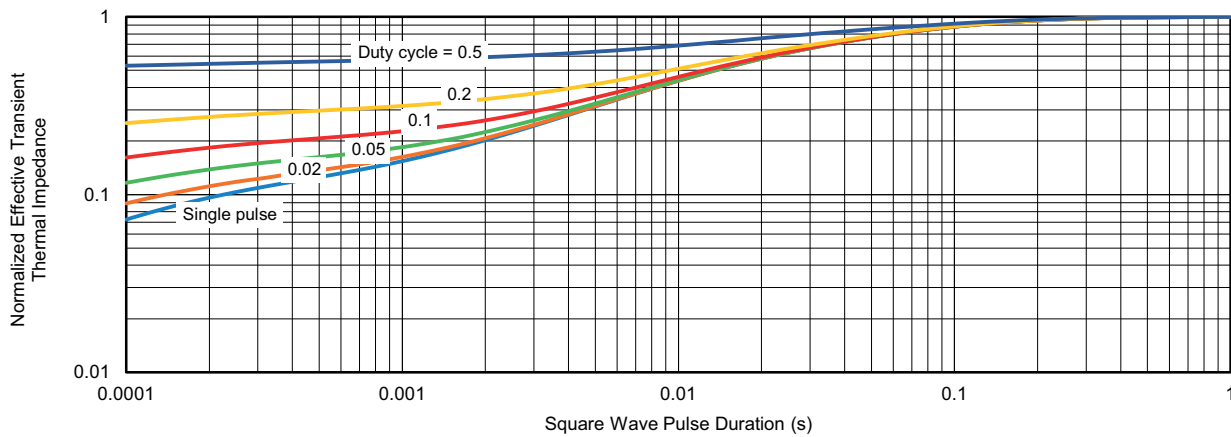
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit
- b.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

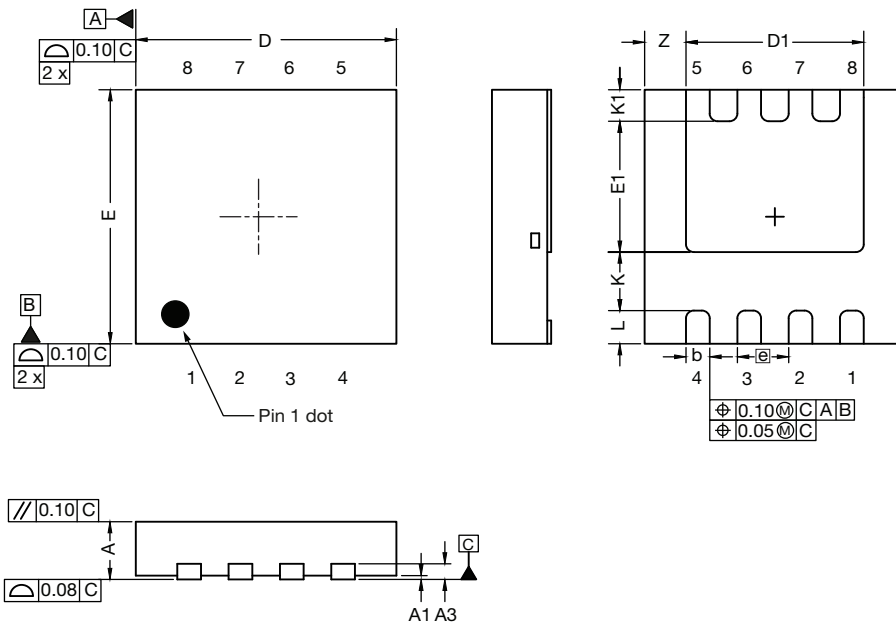


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?77086](http://www.vishay.com/ppg?77086).



### Case Outline for PowerPAK® 1212-SWLH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: C20-0863-Rev. B, 20-Jul-2020  
 DWG: 6062

## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)





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