

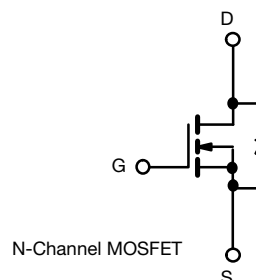
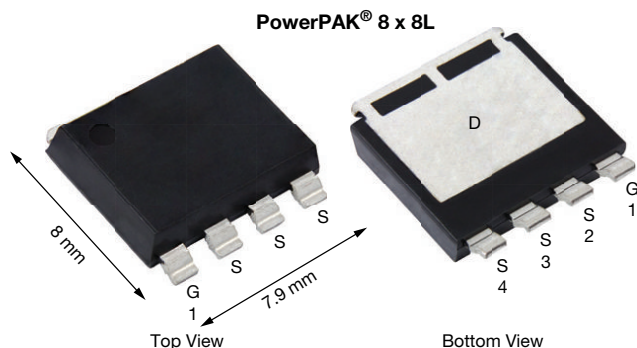
# Automotive N-Channel 80 V (D-S) 175 °C MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Thin 1.6 mm height
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	80
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.0014
I <sub>D</sub> (A)	430
Configuration	Single
Package	PowerPAK 8 x 8L

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	80	V
Gate-source voltage		V <sub>GS</sub>	± 20	
Continuous drain current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	430	A
	T <sub>C</sub> = 125 °C		250	
Continuous source current (diode conduction)		I <sub>S</sub>	450	
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	1200	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	65	mJ
		E <sub>AS</sub>	211	
Maximum power dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	600	W
	T <sub>C</sub> = 125 °C		200	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>c</sup>			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>b</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	0.25	

## Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

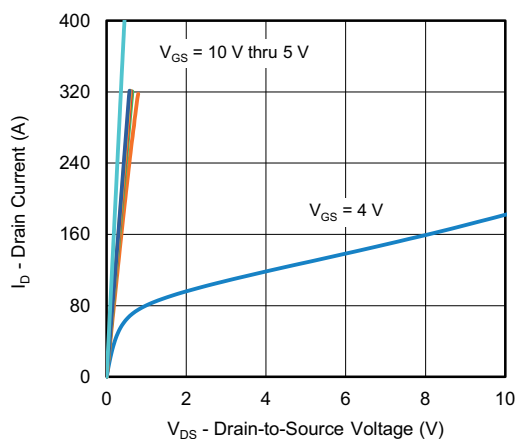
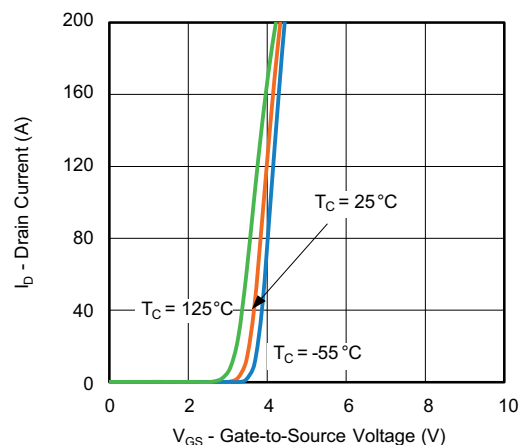
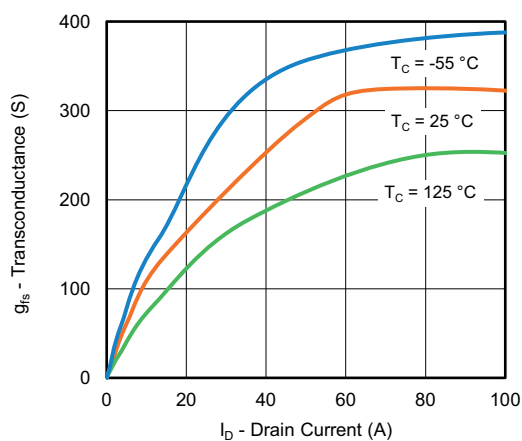
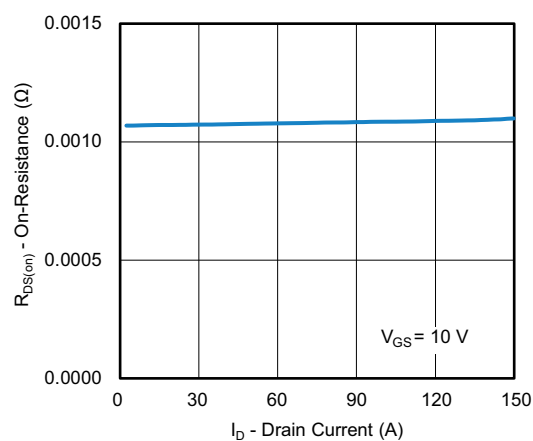
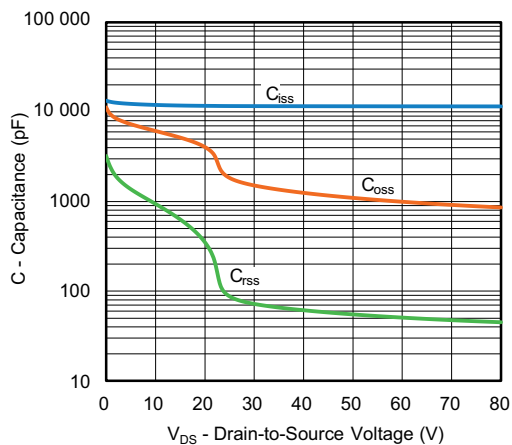
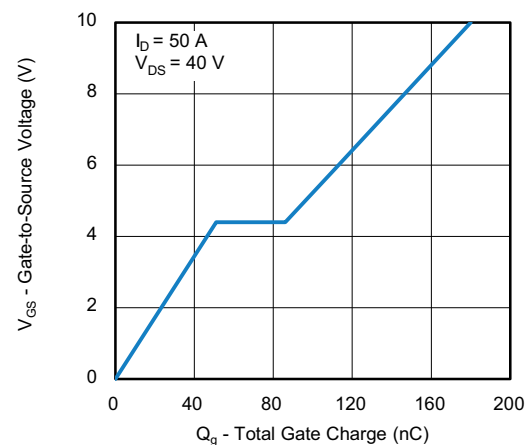


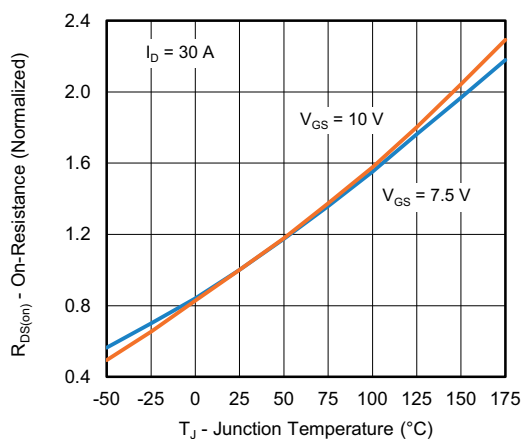
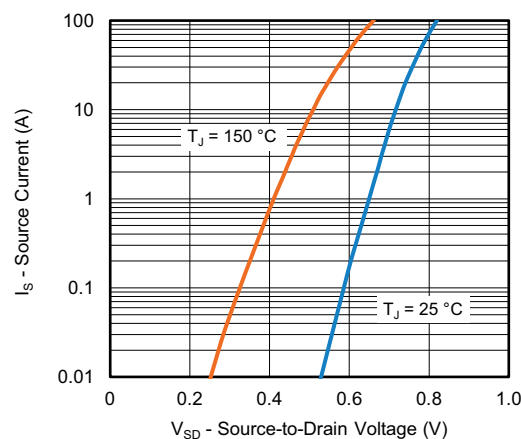
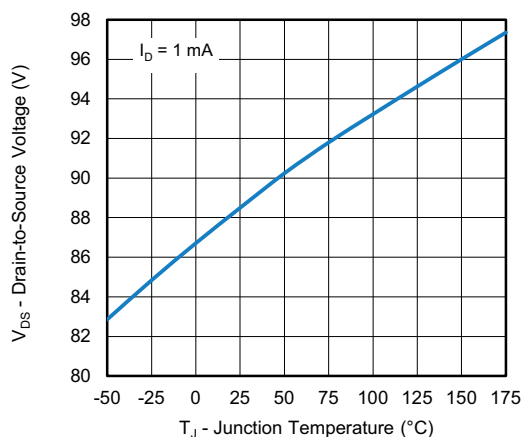
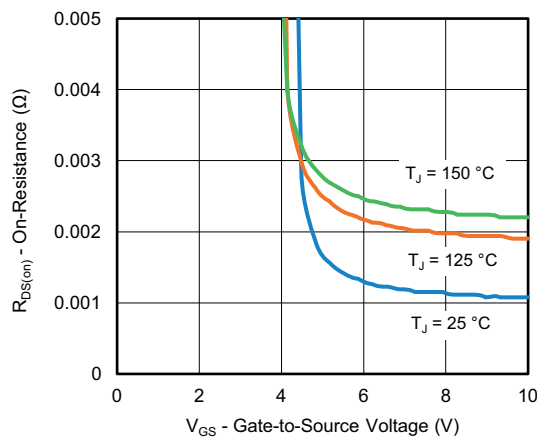
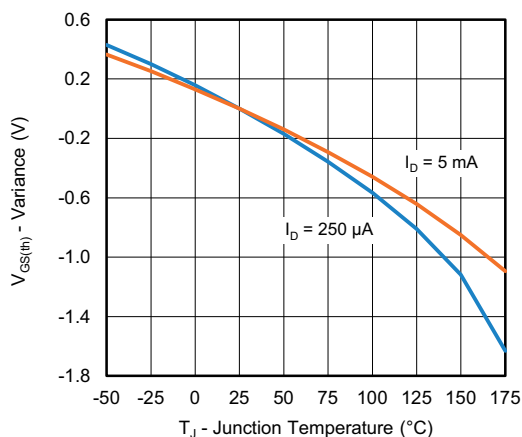
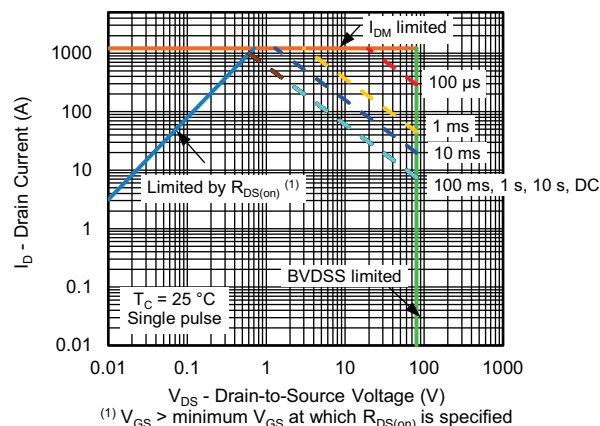
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		80	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	3	3.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 80 V, T <sub>J</sub> = 175 °C	-	-	500	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	50	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.0011	0.0014	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0026	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0033	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		-	82	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	11 435	16 010	pF
Output capacitance	C <sub>oss</sub>			-	1896	2655	
Reverse transfer capacitance	C <sub>rss</sub>			-	92	130	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 50 A	-	181	272	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	51	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	36	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.7	1.3	2	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 0.8 Ω, I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	21	28	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	80	105	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	65	85	
Fall time <sup>c</sup>	t <sub>f</sub>			-	20	28	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	1100	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		-	0.7	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs		-	72	144	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	143	286	nC
Reverse recovery fall time	t <sub>a</sub>			-	41	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	30	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	3.5	-	A

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

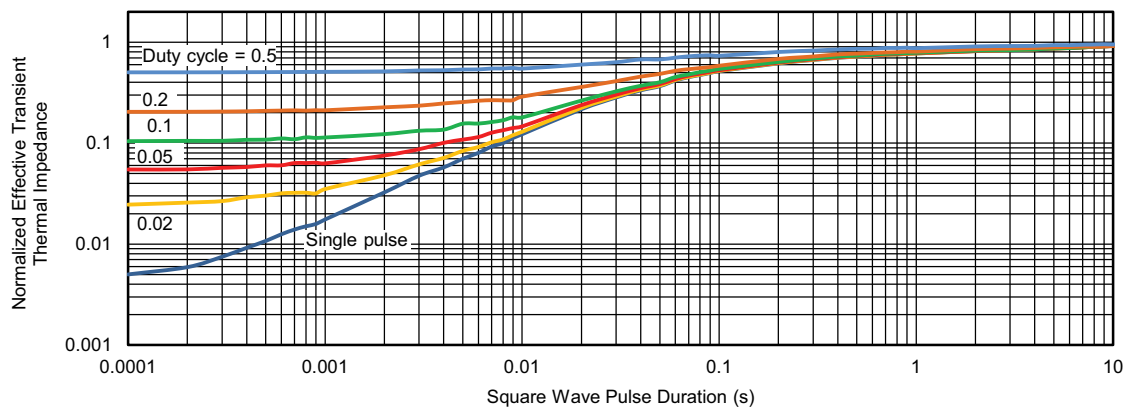
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**Drain Source Breakdown vs. Junction Temperature**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Safe Operating Area**
**Note**

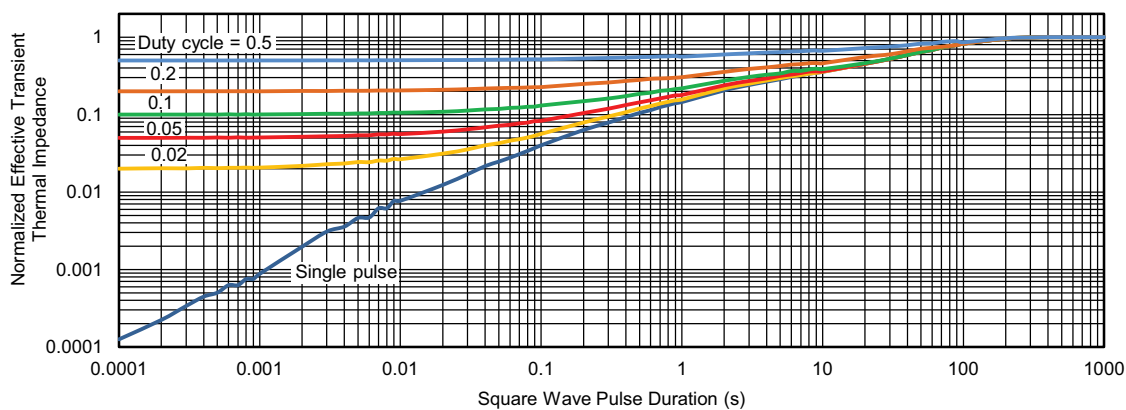
- $V_{GS} > \text{minimum } V_{GS} \text{ at which } R_{DS(on)} \text{ is specified}$



**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



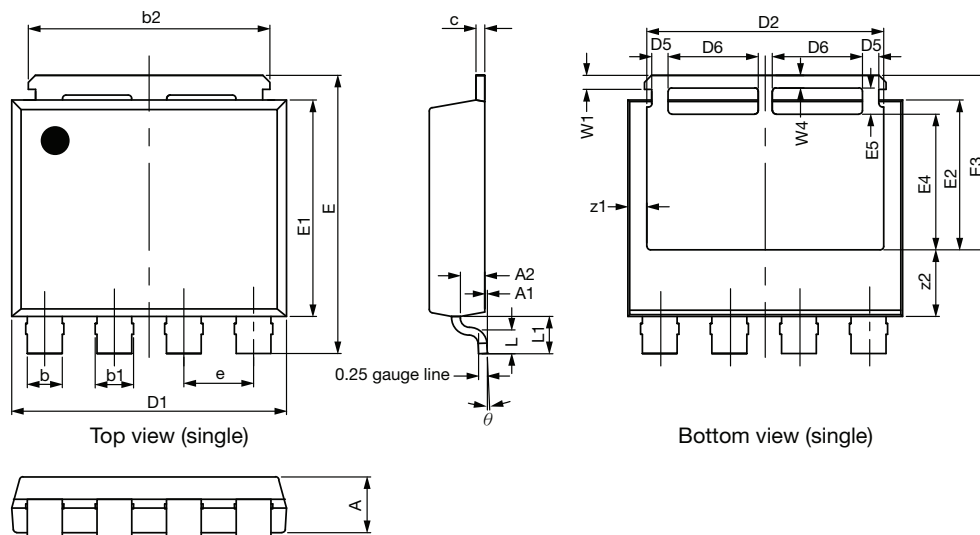
**Normalized Thermal Transient Impedance, Junction-to-Case**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

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## PowerPAK® 8 x 8L BWL Case Outline 2



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
e	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°

ECN: S19-0643-Rev. B, 05-Aug-2019  
DWG: 6073

### Note

- Millimeter will govern



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