

N-Channel 150 V (D-S) MOSFET

DESCRIPTION

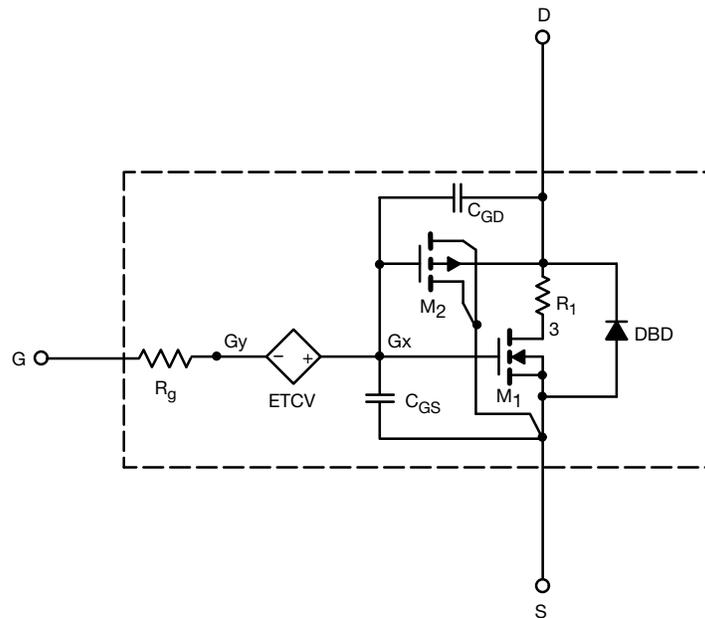
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to 125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



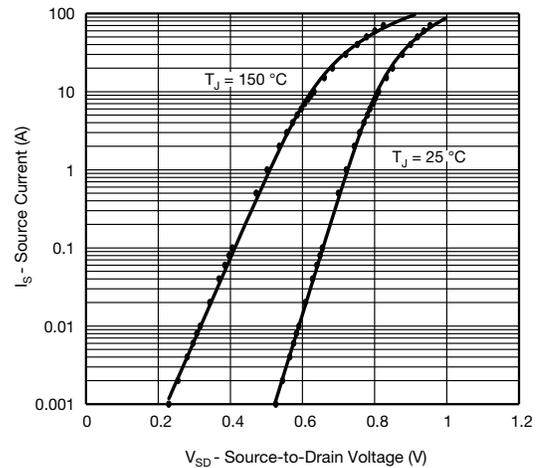
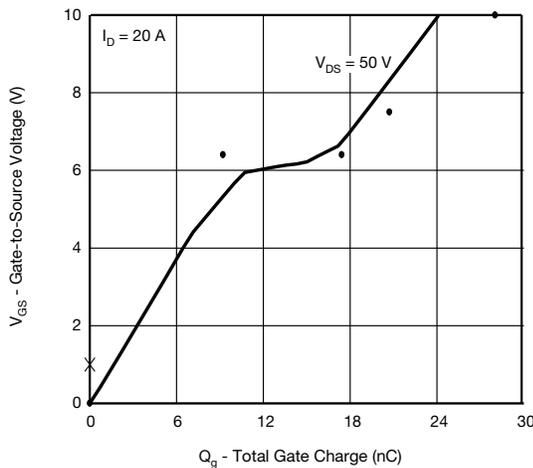
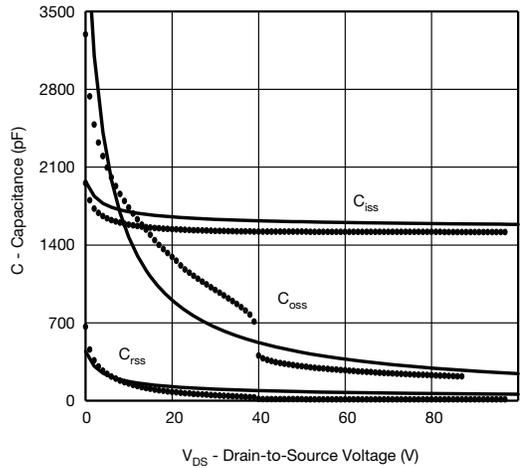
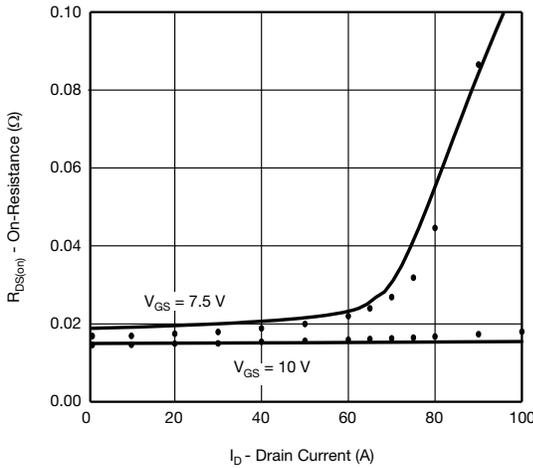
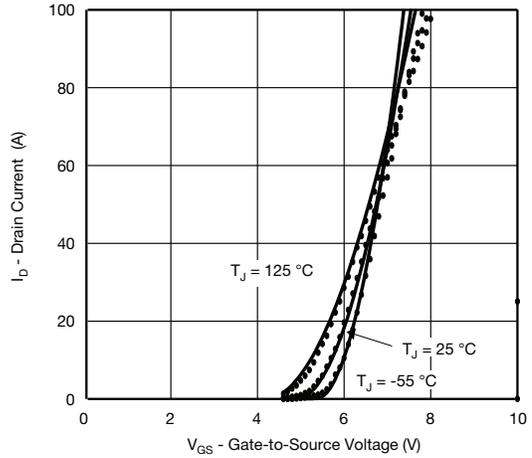
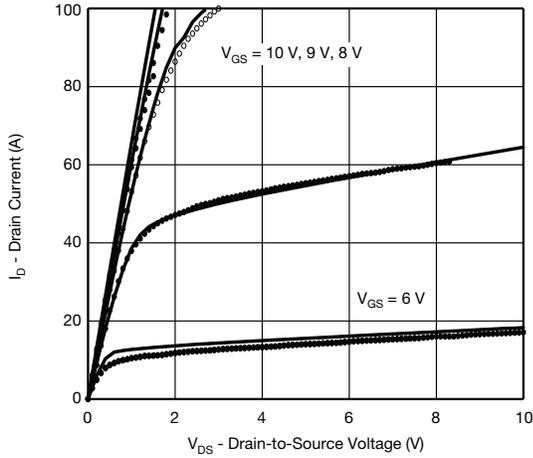
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.9	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	0.0150	0.0147	Ω
		V _{GS} = 7.5 V, I _D = 15 A	0.0191	0.0170	
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A	34	33	S
Diode forward voltage	V _{SD}	I _S = 5 A	0.78	0.77	V
Dynamic ^b					
Input capacitance	C _{iss}	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz	1530	1516	pF
Output capacitance	C _{oss}		253	236	
Reverse transfer capacitance	C _{rss}		11	10.5	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	28	27	nC
Gate-source charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 20 A	21	20.7	
Gate-drain charge	Q _{gd}		9.2	9.2	
			8.2	8.2	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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