P-Channel 60 V (D-S) 175 °C MOSFET

DESCRIPTION

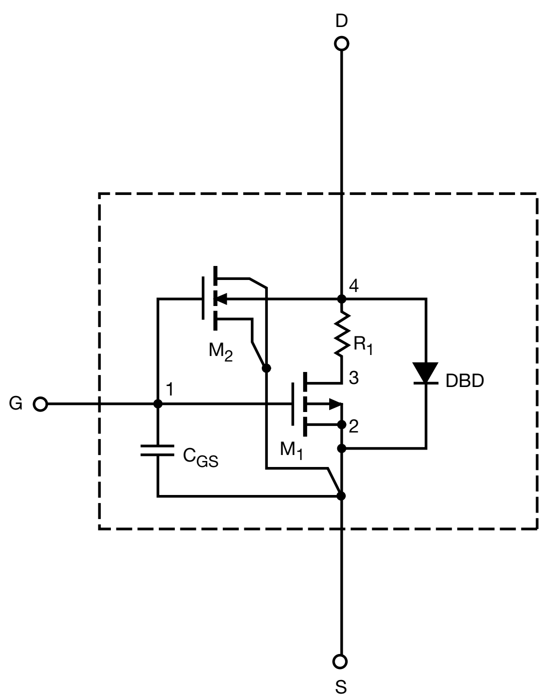
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

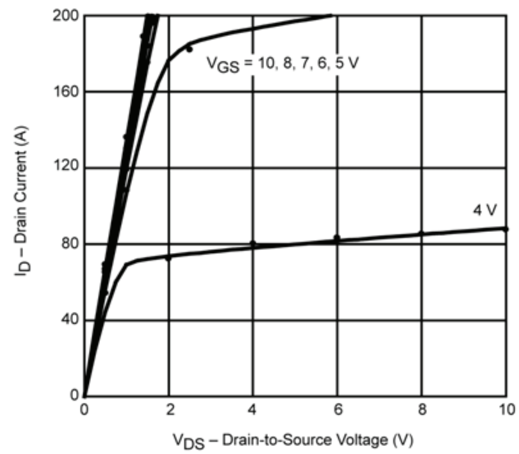
- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

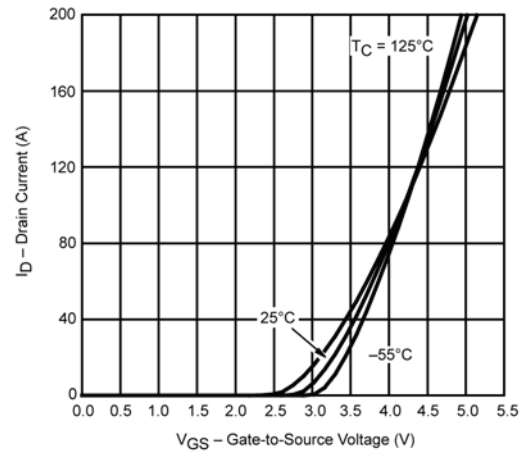
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = -250 µA	2.1	-	V
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	644	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -30 A	0.0074	0.0074	Ω
		V_{GS} = -10 V, I_D = -30 A, T_J = 125 °C	0.0116	-	
		V_{GS} = -10 V, I_D = -30 A, T_J = 175 °C	0.0139	-	
		V_{GS} = -4.5 V, I_D = -20 A	0.0092	0.0094	
Forward Transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -30 A	76	-	S
Diode Forward Voltage [a]	V_{SD}	I_S = -50 A, V_{GS} = 0 V	-0.91	-1	V
Dynamic [b]					
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	8417	9200	pF
Output Capacitance	C_{oss}		970	975	
Reverse Transfer Capacitance	C_{rss}		801	760	
Total Gate Charge	Q_g	V_{DS} = -30 V, V_{GS} = -10 V, I_D = -90 A	176	160	nC
Gate-Source Charge [c]	Q_{gs}		40	40	
Gate-Drain Charge [c]	Q_{gd}		36	36	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -30 V, R_L = 0.33 Ω I_D = -90 A, V_{GEN} = -10 V, R_g = 2.5 Ω	13	20	ns
Rise Time	t_r		255	190	
Turn-Off Delay Time	$t_{d(off)}$		102	140	
Fall Time	t_f		352	300	

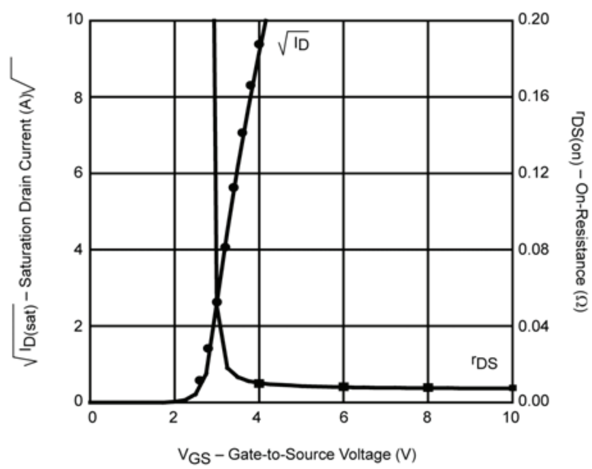
Notes

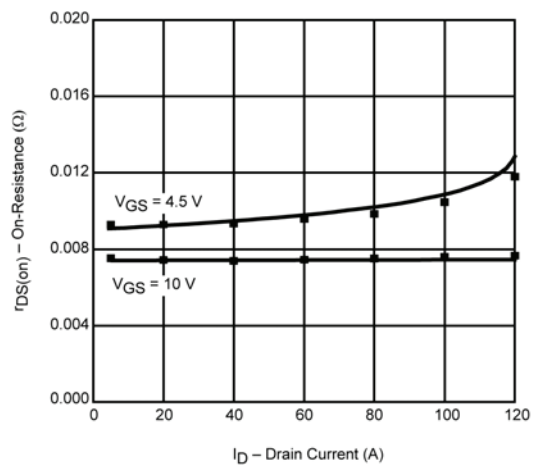
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

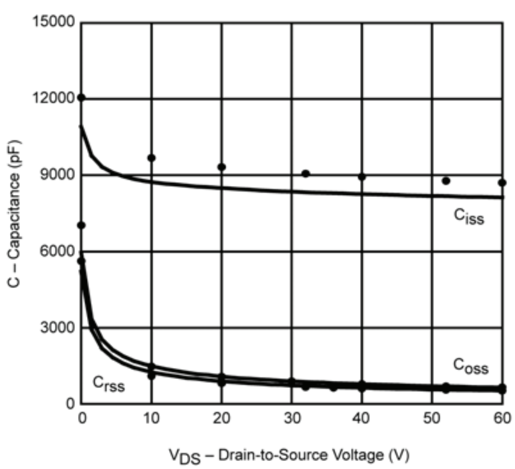
COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)

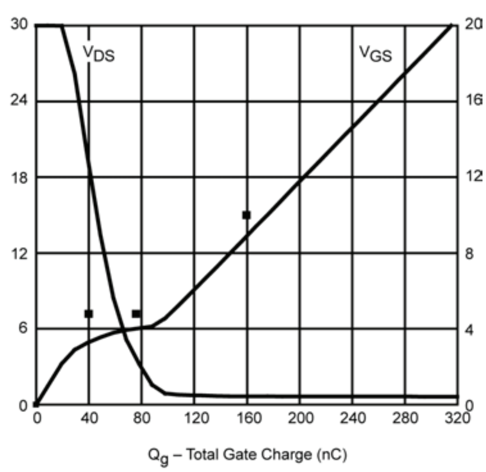












Note

- Dots and squares represent measured data.