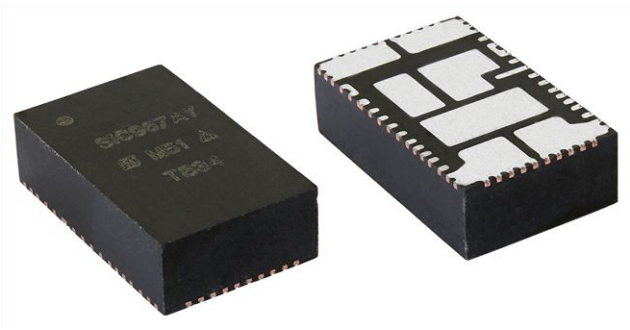
Reference Board User's Manual 4.5 V to 60 V Input, 6 A, DC/DC Synchronous Buck Modules



DESCRIPTION

The SiC967 is a synchronous buck regulator module with integrated power MOSFETs and inductor. Its power stage is capable of supplying 6 A continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.8 V from 4.5 V to 60 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC967's architecture supports ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and no external ESR network is required for loop stability purposes. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output over voltage protection (OVP), cycle by cycle over current protection (OCP) short circuit protection (SCP) and thermal shutdown (OTP). It also has UVLO and 6 ms soft start.

The SiC967 is available in lead (Pb)-free power enhanced PowerPAK® MLP10665-60L package in 10.6 mm x 6.5 mm x 3mm dimensions.

FEATURES

- Versatile
  - Operation from 4.5 V to 60 V input voltage
  - Adjustable output voltage down to 0.8 V
  - Support start-up with pre-bias output voltage
  - ± 1 % output voltage accuracy from -40 °C to +125 °C
- Internal compensation
- Highly efficient
  - 95 % peak efficiency
  - 4 µA supply current at shutdown
  - 100 µA operating current not switching
- Highly configurable
  - Adjustable switching frequency from 100 kHz to 2 MHz
  - Selectable present 100 %, 75 %, and 50 % current limit
  - 2 modes of operation: forced continuous conduction, power save
- Robust and reliable
  - Cycle-by-cycle current limit
  - Output over voltage protection
  - Output under voltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
  - Supported by Vishay PowerCAD online design simulation
- High power density
  - Integration of high current output inductor
  - 10.6 mm x 6.5 mm x 3 mm low profile MLP package
- Easy of use
  - Internal compensation
  - Low peripheral component count
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Industrial and automation
- Home automation
- Industrial and server computing
- Networking, telecom, and base station power supplies
- Wall transformer regulation
- Robotics
- High end hobby electronics: remote control cars, planes, and drones
- Battery management systems
- Power tools
- Vending, ATM, and slot machines

SPECIFICATIONS

This reference board allows the user to evaluate the SiC967 microBUCK® regulators for their features and functionalities. It can also be a reference design for a user's application. The board is configured for 4.5 V to 50 V input. Output current capability is model dependent. The operating range may be modified by changing components such as the mode or feedback resistor.

ORDERING INFORMATION		
BOARD PART NUMBER	MAX. OUTPUT CURRENT	BOARD MARKING
SiC967EVB-A	6 A	UB96A

BOARD CONFIGURATION TABLE

SiC967 EVB TYPICAL PRE-DEFINED OPERATING CONFIGURATIONS			
V_{IN} (V)	V_{OUT} (V)	f_{sw} (kHz)	MAXIMUM I_{OUT} (A)
48.0	3.3	400	6
48.0	5.0	500	6
48.0	12.0	1000	4

CONNECTION AND SIGNAL / TEST POINTS

Power Terminals (J4)

- **V_{IN}, GND (J4, pin 1 and pin 2):** (see Fig. 1)

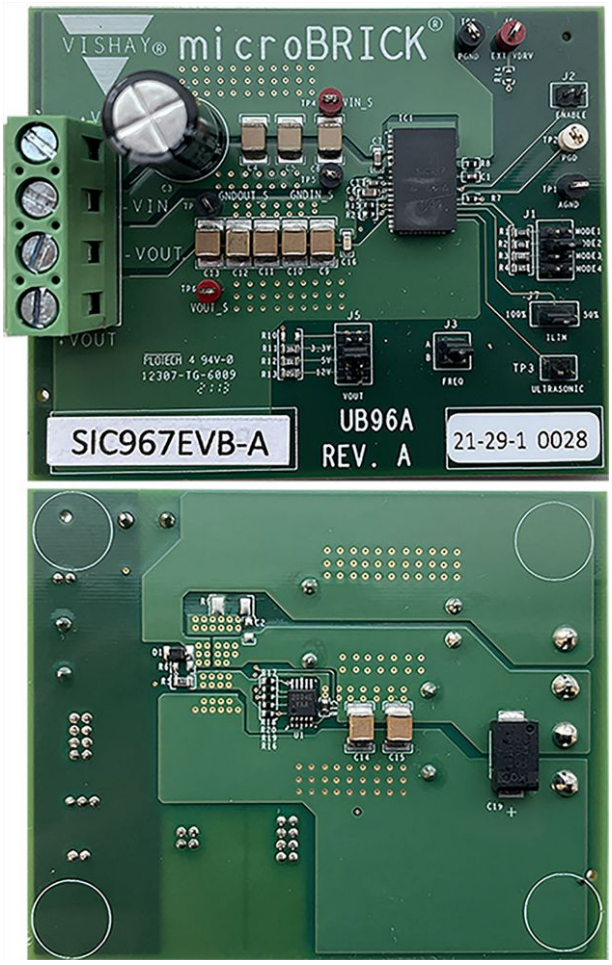


Fig. 1 - SiC967 EVB

Connect to a voltage source: 36 V to 50 V. This reference board configures 32 V as the minimal value of input voltage to enable the chip, and 27 V as the input voltage's under-voltage lockout (V_{IN} UVLO) voltage.

Both values can be modified by changing resistance of R6 using the equation in (1) and (2).

$$R6 = \frac{(PVIN_{EN} - 1.4) \times R5}{1.4} \quad (1)$$

where $PVIN_{EN}$ is the level of input voltage, in volts, enabling the chip, R5 is the resistance of resistor R5 populated as 2 kΩ on this reference board.

$$PVIN_{UVLO} = 1.2 \times \frac{(R5 + R6)}{R5} \quad (2)$$

where $PVIN_{UVLO}$ is the level of input voltage, in volts, applying VIN UVLO protection.

EVB provides another option to configure V_{IN} UVLO by removing R6 and populate a Zener diode D1 on board. In this case, $PVIN_{EN}$ will be 1.4 V above reverse breakdown voltage of D1.

The minimum value of $PVIN_{EN}$ has to be 4.4 V, which shall be higher than V_{DD} UVLO threshold voltage.

- **V_{OUT}, GND (J4, pin 3 and pin 4):** (see Fig. 1)

Connect to a load that draws no more than 6A.

The output voltage is selectable on J5.

Note

- The output capacitors are rated to 25 V. Should a higher output voltage be required, the output capacitors should be changed to ones with an appropriate higher voltage rating

SELECTION JUMPERS

Operation Mode Select Using J1 and TP3

J1 allows the user to select modes of power saving and whether using an internal LDO regulator or an external power supply as V_{DRV} for operation.

TP3 is reserved for future use, please always leave the jumper open.

The Table below lists all modes of operation and their related jumper setup.

OPERATION MODES				
MODE	POWER SAVE MODE	V_{DRV} SUPPLY	J1 JUMPER SETUP (FOLLOWING SILKSCREEN LABEL)	TP3 JUMPER SETUP
1	Enabled	Internal LDO	Pin 1 - 2 shorted	Open
2	Disabled	Internal LDO	Pin 3 - 4 shorted	Open
3	Disabled	External supply	Pin 5 - 6 shorted	Open
4	Enabled	External supply	Pin 7 - 8 shorted	Open

V_{DRV} External Supply

5 V (J6), GND (TP8): this is the terminal that enables the user to use an external 5 V_{DC} supply as MOSFET gate driver supply when mode 3 or 4 in Table "Operation Mode" is selected. This should only be used in mode 3 and 4.

Enable

J2 is a 2 pin header crossing EN pin to ground. The EN pin has an internal high impedance pull down resistor and requires a DC voltage higher than 1.43 V to enable chip operation. Shorting **J2** with a jumper will disable the chip operation.

Output Voltage V_{OUT} Setting

J5 allows the user to choose four options of output voltage divider to set different output voltage V_{OUT}. **J5** is a 4 x 2 eight pin header and table "Output Voltage Setting" lists the available voltage setting and related jumper setup. The user can use equation in datasheet to calculate required resistance for a designated output voltage, where R13 resistance is 10.2 kΩ.

OUTPUT VOLTAGE SETTING		
V_{OUT} DESIRED (V)	J5 JUMPER SETUP (FOLLOWING SILKSCREEN LABEL)	RESISTANCE BETWEEN V_{OUT} AND FB PIN (kΩ)
Customized	Pin 1 - 2 shorted	Customized
3.3	Pin 3 - 4 shorted	31.6
5.0	Pin 5 - 6 shorted	53.6
12.0	Pin 7 - 8 shorted	143

Switching Frequency f_{sw} Setting

J3 allows the user to choose correct resistance to achieve 300 kHz switching frequency after the users set up output voltage following table "Output Voltage Setting".
J3 is a 2 x 2 four pin header and it generates logic level of input pins of **U1** (DG2034, multiplexers). Table "Switching Frequency Setting" lists the related logic level of **U1** matching different output voltages in table "Output Voltage Setting" and related **J3** jumper setup. The user can use equation in datasheet to calculate required resistance to achieve a desired switching frequency with a designated output voltage.

SWITCHING FREQUENCY SETTING				
SWITCHING FREQUENCY DESIRED (kHz)	V_{OUT} (V) (1)	U1 INPUT LOGIC	J3 JUMPER SETUP	RESISTANCE BETWEEN f_{sw} AND GND (kΩ)
400	3.3	2'b01	Pin 1 - 3 shorted (A)	43.2
500	5.0	2'b10	Pin 2 - 4 shorted (B)	52.3
n/a	n/a	2'b00	All pins leave open	n/a
1000	12.0	2'b11	Both Pin 1 - 3 (A) and Pin 2 - 4 (B) shorted	63.4

Note

(1) V_{OUT} set in table "Output Voltage Setting"

Maximum Inductor Valley Current Limit I_{LM} Setting

J7 allows the user to choose three options of the maximum inductor valley current limit. **J7** is a 3 x 1 three pins header and its middle pin (Pin 2) connects to number 31 pin I_{LIMIT} of IC1. Pin 1 of **J7** is facing IC1 with silkscreen label "100 %", and Pin 3 of **J7** is facing the EVB edge with silkscreen label "50 %". Table "Maximum Valley Current Limit" lists the three optional values of the maximum valley current limit and their related jumper setup.

MAXIMUM VALLEY CURRENT LIMIT SETTING		
I_{OCP} (A)	J7 JUMPER SETUP	IC1 I_{LIMIT} PIN CONNECTION
10	Pin 2 - 1 shorted	I_{LIMIT} tied to V_{DD}
7.5	Three pins leave open	I_{LIMIT} is not connected
5	Pin 2 - 3 shorted	I_{LIMIT} tied to A_{GND}

SIGNALS AND TEST LEADS

Input Voltage Sense

V_{IN_SENSE} (TP4), GND_{IN_SENSE} (TP5): this allows the user to measure the voltage directly at the input of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of a power source with remote sense capability.

Output Voltage Sense

V_{OUT_SENSE} (TP6), GND_{OUT_SENSE} (TP7): This allows the user to measure the output voltage directly at the sense point of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of an external load with remote sense capability.

Power Good Indicator

P_{GOOD}: is an open drain output and is pulled up with a 102 kΩ resistor, R7, to V_{DD} (5 V). When FB or V_{OUT} are within -10 % to +20 % of the set voltage this pin will go HI to indicate the output is okay.

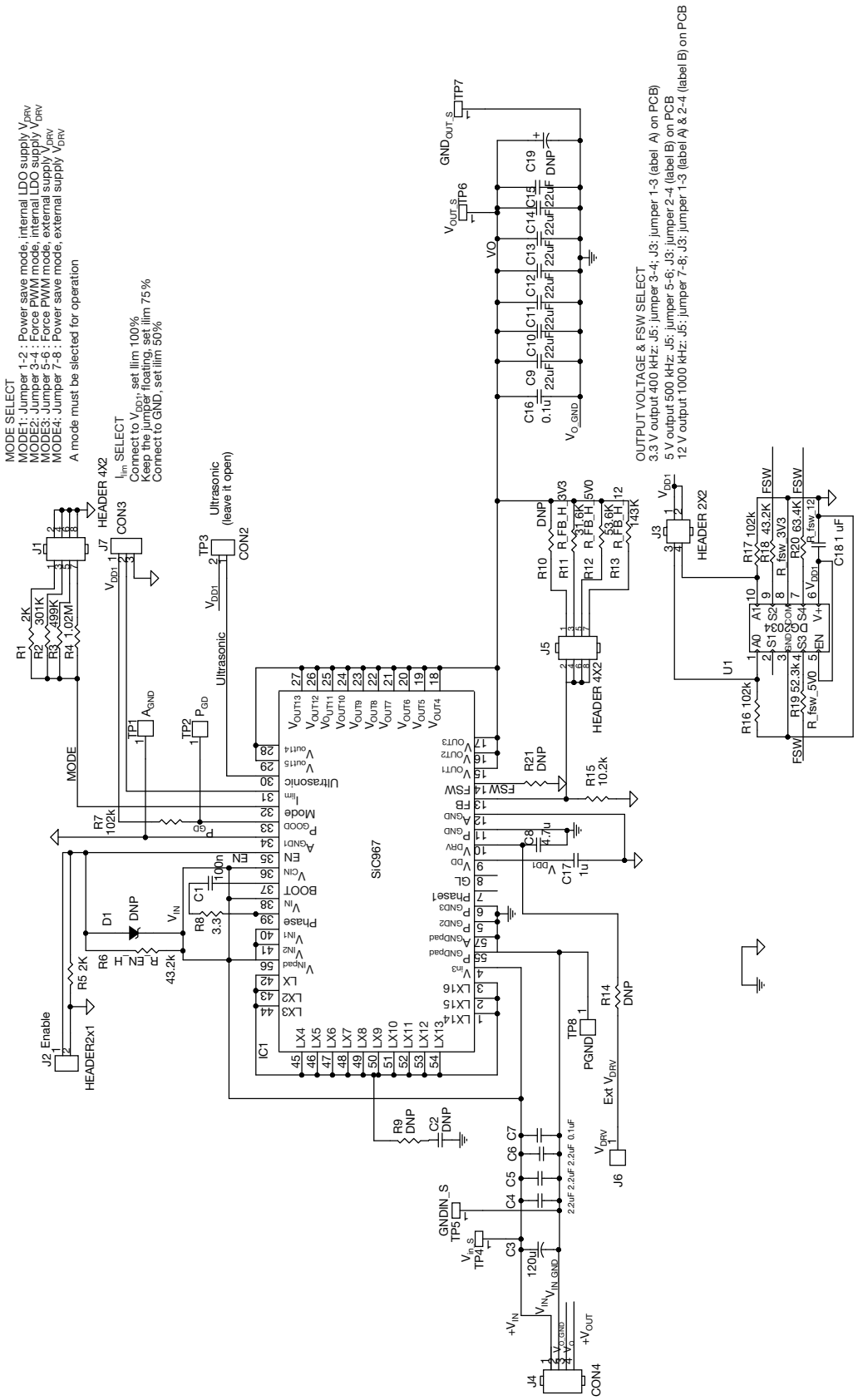
Power Up Procedure

Before turning on the reference board, the user needs to select one of the four modes by shorting one jumper (see section on mode selection). If mode 3 or 4 is selected, make sure V_{DRV} pin is supplied by external 5 V. There is no specific power sequence requirement to power up the board.

Snubber Circuit

Snubber may be used when the user desire to decrease the peak voltage of switching node SW during turn on of the high side switch. There are place holders on the reference board R9 and C2 for the snubber.

SCHEMATIC FOR SiC967



PCB LAYOUT FOR SiC967

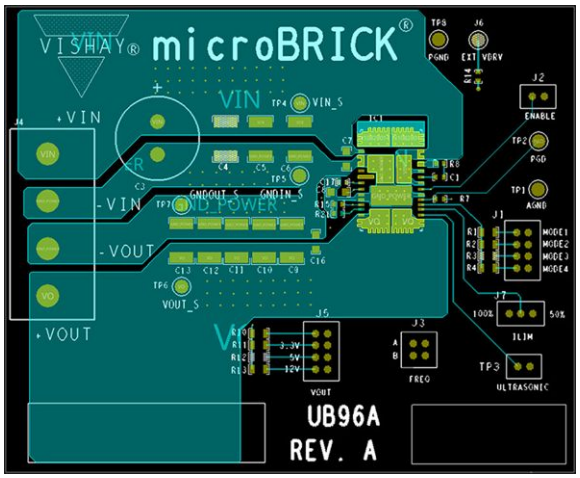


Fig. 2 - Top Layer

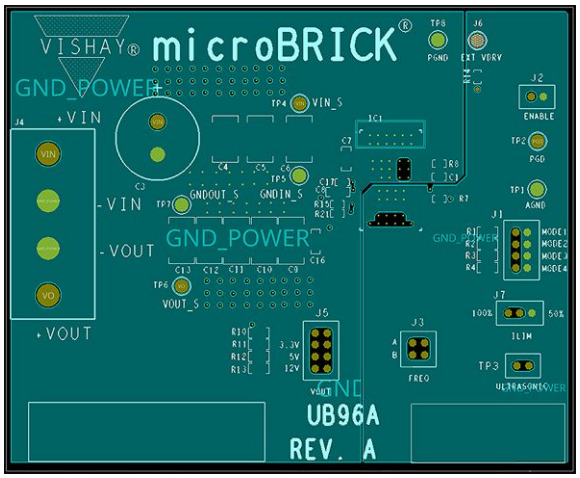


Fig. 3 - Inner Layer 2

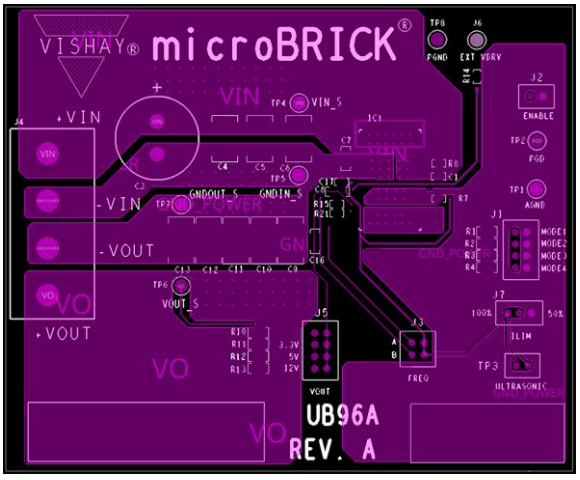


Fig. 4 - Inner Layer 3

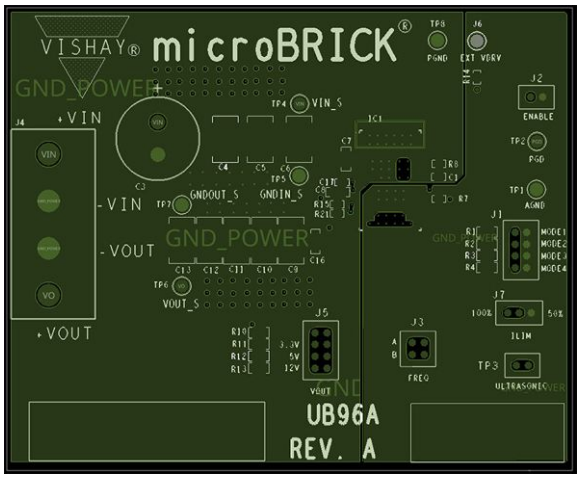


Fig. 5 - Inner Layer 4

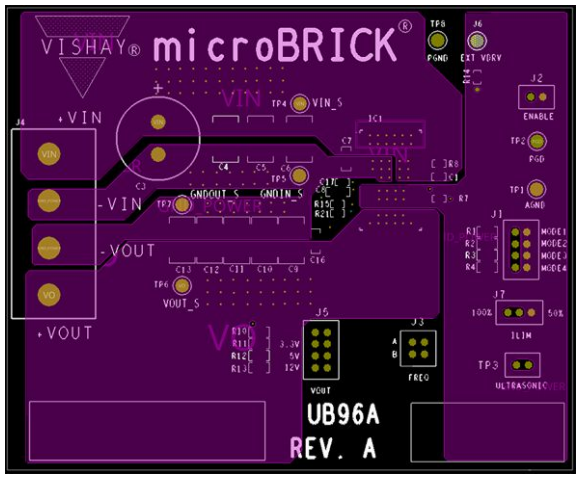


Fig. 6 - Inner Layer 5

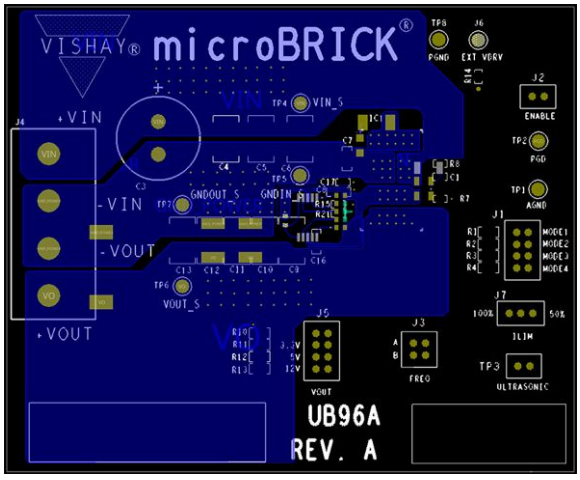


Fig. 7 - Bottom Layer

BILL OF MATERIAL REPORT FOR SiC967

BOM FOR SIC967		QTY	REFERENCE DESIGNATOR
PART NUMBER	DESCRIPTION		
VJ0603Y104KXAAC	0.1 µF ±10 % 50 V X7R 0603	2	C1, C16
	DNP	0	C2
EEU-FS1J121LB	CAP ALUM 120UF 20 % 63 V thru hole	1	C3
GCJ32DR72A225KA01L	2.2 µF ±10 % 100 V X7R 1210	3	C4, C5, C6
GRM188R72A104MA35D	0.1 µF ±10 % 100 V X7R 0603	1	C7
VJ0603G475KXJCW1BC	4.7 µF ±10 % 16 V X5R 0603	1	C8
GRM32ER71E226KE15L	22 µF ±10 % 25 V X7R 1210	7	C9, C10, C11, C12, C13, C14, C15
GRT155R61E105KE01D	1 µF ±10 % 25 V X5R 0402	2	C17, C18
	DNP	0	C19
	DNP	0	D1
SiC967	microBRICK™ 60 V DC/DC converter 6 A	1	IC1
GRPB042VWVN-RC	CONN HEADER VERT 8POS 1.27 mm	2	J1, J5
GRPB021VWVN-RC	CONN HEADER VERT 2POS 1.27 mm	1	J2
GRPB022VWVN-RC	CONN HEADER VERT 4POS 1.27 mm	1	J3
ED120/4DS	TERM BLK 4P SIDE ENT 5.08 mm PCB	1	J4
36-5002-ND	Test point, white	1	J6
GRPB031VWVN-RC	CONN HEADER VERT 3POS 1.27 mm	1	J7
CRCW06032K00FKEAC	RES SMD 2 kΩ 1 % , 1/10 W 0603	2	R1, R5
CRCW0603301KFKEA	RES SMD 301 kΩ 1 %, 1/10 W 0603	1	R2
CRCW0603499KFKEA	RES SMD 499 kΩ 1 %, 1/10 W 0603	1	R3
CRCW06031M02FKEA	RES SMD 1.02 mΩ 1 %, 1/10 W 0603	1	R4
CRCW060343K2FKEA	RES SMD 43.2 kΩ 1 %, 1/10 W 0603	2	R6, R18
CRCW0603102KFKEA	RES SMD 102 kΩ 1 %, 1/10 W 0603	3	R7, R16, R17
CRCW06033R30FKEA	RES SMD 3.3 Ω 1 %, 1/10 W 0603	1	R8
	DNP	0	R09, R10, R14, R21
CRCW060331K6FKEA	RES SMD 31.6 kΩ 1 %, 1/10 W 0603	1	R11
CRCW060353K6FKEA	RES SMD 53.6 kΩ 1 %, 1/10 W 0603	1	R12
CRCW0603143KFKEA	RES SMD 143 kΩ 1 %, 1/10 W 0603	1	R13
CRCW060310K2FKEA	RES SMD 10.2 kΩ 1 %, 1/10 W 0603	1	R15
CRCW060352K3FKEA	RES SMD 52.3 kΩ 1 %, 1/10 W 0603	1	R19
CRCW060363K4FKEA	RES SMD 63.4 kΩ 1 %, 1/10 W 0603	1	R20
36-5001-ND	Test point, black	4	TP1, TP5, TP7, TP8
36-5002-ND	Test point, white	2	TP2
	DNP	0	TP3
36-5000-ND	Test point, rED	2	TP4, TP6
DG2034EDQ-T1-GE3	IC SWITCH SP4T SINGLE 10MSOP	1	U1
NPB02SVFN-RC	CONN jumper shorting 1.27 mm	6	Off board x 6
UB96A	SiC967 EVB	1	PCB