SPICE Device Model SiSS42DN



Vishay Siliconix

N-Channel 100 V (D-S) MOSFET

DESCRIPTION

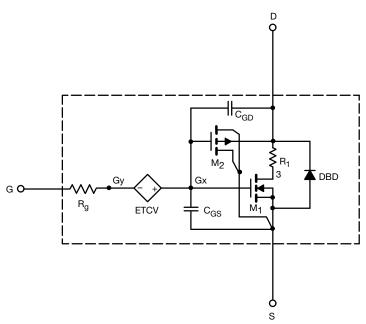
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched Cgd model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over the -55 °C to 125 °C temperature range
- · Model the gate charge



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\;\mu A$	3	-	V
Drain-source on-state resistance ^a	Р	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	0.012	0.012	Ω
	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	0.013	0.013	
Forward transconductance ^a	g fs	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	43	46	S
Diode forward voltage	V _{SD}	I _S = 5 A	0.77	0.77	V
Dynamic ^b			•		
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	1880	1850	pF
Output capacitance	C _{oss}		164	154	
Reverse transfer capacitance	C _{rss}		17	12	
Total gate charge	0	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	24.7	24.8	nC
	Qg	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 7.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	18.6	18.9	
Gate-source charge	Q _{gs}		7.4	7.4	
Gate-drain charge	Q _{gd}		3.8	3.8	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$

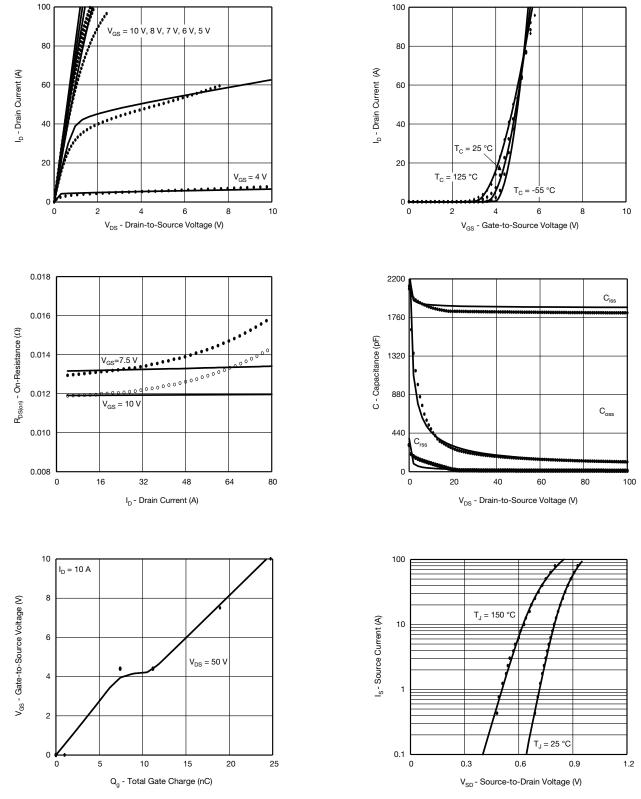
b. Guaranteed by design, not subject to production testing

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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.

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