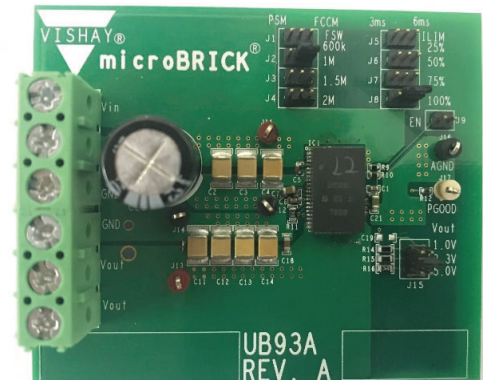
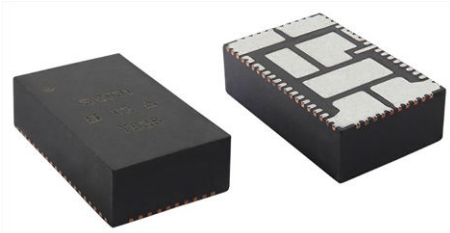
Reference Board User's Manual
High Current Synchronous Buck Modules





DESCRIPTION

The SiC931 is a synchronous buck regulator module with integrated power MOSFETs and inductor. Its power stage is capable of supplying 20 A continuous current at up to 2 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 3 V to 18 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiC931's architecture supports ultrafast transient response with minimum output capacitance and tight ripple regulation at very light load. The device is internally compensated and no external ESR network is required for loop stability purposes. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The regulator integrates a full protection feature set, including output over voltage protection (OVP), cycle by cycle over current protection (OCP), short circuit protection (SCP), and thermal shutdown (OTP). It also has UVLO and a user programmable soft start.

The SiC931 is available in lead (Pb)-free power enhanced PowerPAK® MLP10665-60L package in 10.6 mm x 6.5 mm.

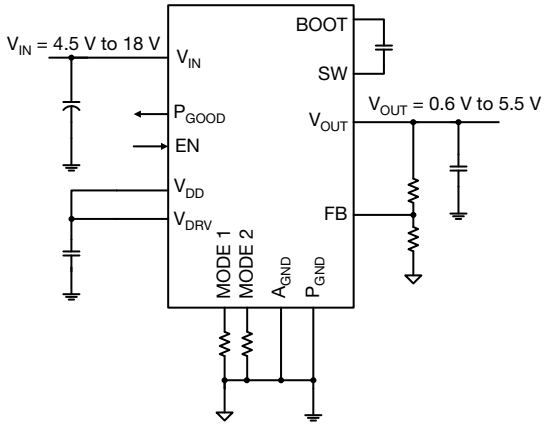
APPLICATIONS

- 5 V, 12 V, and 18 V input rail POLs
- Desktop, notebooks, server, and industrial computing
- Industrial and automation
- Consumer electronics

FEATURES

- Versatile
  - Operation from 3 V to 18 V input voltage
  - Adjustable output voltage down to 0.6 V
  - Support start-up with pre-bias output voltage
  - ± 1 % output voltage accuracy from -40 °C to +125 °C
- Highly efficient
  - 95 % peak efficiency
  - 1 µA supply current at shutdown
  - 50 µA operating current, not switching
- Highly configurable
  - Four programmable switching frequencies available: 600 kHz, 1 MHz, 1.5 MHz, and 2 MHz
  - Adjustable soft start and adjustable current limit
  - Two modes of operation: forced continuous conduction, power save
- Robust and reliable
  - Cycle-by-cycle current limit
  - Output overvoltage protection
  - Output undervoltage / short circuit protection with auto retry
  - Power good flag and over temperature protection
- High power density
  - Integration of high current output inductor
  - 10.6 mm x 6.5 mm x 3 mm low profile MLP package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATIONS CIRCUIT AND PACKAGE OPTIONS



SPECIFICATIONS

This reference board allows the end user to evaluate the SiC931 product chips for its features and all functionalities. It can also be served as a reference design for a user's application.

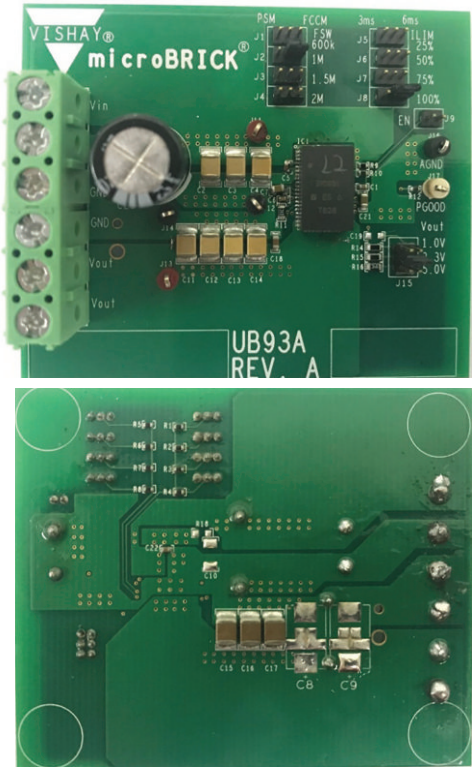


Fig. 1 - SiC931 EVB

BOARD CONFIGURATION TABLE

SiC931 EVB TYPICAL PRE-DEFINED OPERATING CONFIGURATIONS (1)			
V_{IN} (V)	V_{OUT} (V)	f_{sw} (kHz)	MAXIMUM I_{OUT} (A)
12.0	1.0	600	20
12.0	3.3	1000	20
12.0	5.0	1500	18

Note

(1) Output voltage V_{OUT} is set by J15 jumper; switching frequency f_{sw} and switching mode is set by J1, J2, J3, and J4 specified in table "Mode 1"; soft start time and OCP percentage is set by J5, J6, J7, and J8 specified in table "Mode 2"; 200 LFM airflow is recommended for SiC931 EVB when loading the maximum I_{OUT} current

CONNECTION AND SIGNAL / TEST POINTS

Power Terminal

V_{IN} (J10 - #1), GND (J10 - #2)

Connect a voltage source to this terminal. The minimum input voltage will be 3 V. For input voltages (V_{IN}) below 4.5 V, an external V_{DD} and V_{DRD} is required.

V_{OUT} (J10 - #5, #6), GND (J10 - #3, #4)

Connect an electronic load to this terminal.

SELECTION JUMPERS

Enable of Device

J9: this is the jumper that enables / disables the part. With J9 two pins left open, the device is enabled. With J9 two pins shorted, the device is disabled.

Output Voltage V_{OUT} Setting

J15: this is the jumper that select output voltage. J15 is a 3 x 2 six-pin header illustrated in Fig. 2. Shorting two pins in a row, from top to bottom as indicated in Fig. 2, output voltage V_{OUT} can be set to 1.0 V, 3.3 V, or 5.0 V. An example setup illustrated in Fig. 2 is 3.3 V. The default setup is 1.0 V.

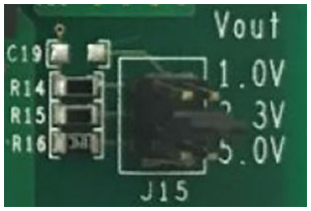


Fig. 2 - J15 Jumper on EVB for Output Voltage Setting

Mode 1 Select

J1, J2, J3, and J4 are four 1 x 3 three-pin headers which allow user to select one option out of sixteen choices of switching frequency f_{sw} and mode of operation. Table "Mode 1" specifies all options to achieve by setting **J1, J2, J3, and J4**. The left pin is defined as the left most pin of the 1 x 3 header closer to Vishay logo on EVB. The right pin is defined as the right most pin of the 1 x 3 header far from the Vishay logo on EVB. The middle pin is defined as the pin of the 1 x 3 header sitting between the left pin and the right pin.

MODE 1 OPTIONS FROM SETTING J1, J2, J3, AND J4			
NO	f_{SW} (kHz)	MODE OF OPERATION	JUMPER SETUP ON J1, J2, J3, AND J4
1	600	FCCM	The right pin of J1 shorted to the middle pin of J1; all other pins keeps open
2	600	PSM	The left pin of J1 shorted to the middle pin of J1; all other pins keeps open
3 (1)	1000	FCCM	The right pin of J2 shorted to the middle pin of J2; all other pins keeps open
4	1000	PSM	The left pin of J2 shorted to the middle pin of J2; all other pins keeps open
5	1500	FCCM	The right pin of J3 shorted to the middle pin of J3; all other pins keeps open
6	1500	PSM	The left pin of J3 shorted to the middle pin of J3; all other pins keeps open

MODE 1 OPTIONS FROM SETTING J1, J2, J3, AND J4			
NO	f_{SW} (kHz)	MODE OF OPERATION	JUMPER SETUP ON J1, J2, J3, AND J4
7	2000	FCCM	The right pin of J4 shorted to the middle pin of J4; all other pins keeps open
8	2000	PSM	The left pin of J4 shorted to the middle pin of J4; all other pins keeps open

Note

(1) Default setup on EVB

Mode 2 Select

J5, J6, J7, and J8 are four 1 x 3 three-pin headers which allow user to select one option out of sixteen choices of soft start time and OCP's percent over its maximum value. Table "Mode 2" specifies all options to achieve by setting **J5, J6, J7, and J8**. The left pin is defined as the left most pin of the 1 x 3 header closer to Vishay logo on EVB. The right pin is defined as the right most pin of the 1 x 3 header far from the Vishay logo on EVB. The middle pin is defined as the pin of the 1 x 3 header sitting between the left pin and the right pin.

MODE 2 OPTIONS FROM SETTING J5, J6, J7, AND J8			
NO	SOFT START (ms)	OCP (%)	JUMPER SETUP ON J5, J6, J7, AND J8
1	6	25	The right pin of J5 shorted to the middle pin of J5; all other pins keeps open
2	3	25	The left pin of J5 shorted to the middle pin of J5; all other pins keeps open
3	6	50	The right pin of J6 shorted to the middle pin of J6; all other pins keeps open
4	3	50	The left pin of J6 shorted to the middle pin of J6; all other pins keeps open
5	6	75	The right pin of J7 shorted to the middle pin of J7; all other pins keeps open
6	3	75	The left pin of J7 shorted to the middle pin of J7; all other pins keeps open
7 (1)	6	100	The right pin of J8 shorted to the middle pin of J8; all other pins keeps open
8	3	100	The left pin of J8 shorted to the middle pin of J8; all other pins keeps open

Note

(1) Default setup on EVB

PV_{IN} ENHANCED UVLO OPTION

SiC931 uses LDO circuit to generate internal V_{DD} from PV_{IN}, so its V_{DD} UVLO feature may be used to implement PV_{IN} UVLO like the EVB did. In cases that an enhanced PV_{IN}UVLO feature may be required in those applications where either the level of PV_{IN} UVLO is higher than 4 V or avoiding SiC931 falsely turn on during extreme PV_{IN} crashing is required, the user has an option to modify the EVB and use EN hysteresis to realize an enhanced PV_{IN} UVLO feature.

The user needs to change R9 from 100 kΩ to 20 kΩ, then add a resistor and a capacitor 0.1 µF (50 V rating) in the schematic and BOM, where two components are connected from EN to ground. For the EVB, the user may populate the two components on the bottom side of EVB crossing two pins of J9. Equation (1) lists an equation for the user to calculate the resistance of the added resistor.

$$R99 = \frac{R9}{(PVIN_{EN\_H} - 1{,}0)} \quad (1)$$

, where $PVIN_{EN\_H}$ is the expected level of PV_{IN}, in volts, enabling SiC931, R9 is resistance of the resistor R9, R99 is resistance of the resistor to be added between EN and ground.

For example, provided that $PVIN_{EN\_H}$ is chosen as 7.6 V and R9 is 20 kΩ, the calculated resistance of R99 is 3.03 kΩ and a 3.01 kΩ resistor shall be selected following E96 table.

SIGNALS AND TEST LEADS

Input Voltage Sense

V_{IN_SENSE} (J11), GND_{IN_SENSE} (J12): this allows the user to measure the voltage directly at the input of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of a power source with remote sense capability.

Output Voltage Sense

V_{OUT_SENSE} (J13), GND_{OUT_SENSE} (J14): this allows the user to measure the output voltage directly at the sense point of the regulator bypassing any losses generated by connections to the board. These test points can also be as a remote sense port of an external load with remote sense capability.

Power Good Indicator

P_{GOOD} (J17): is an open drain output and is pulled up with a 100 kΩ resistor, R12, to V_{DD1} (5 V). When FB or V_{OUT} are within -10 % to +20 % of the set voltage this pin will go HI to indicate the output is okay. To prevent false triggering during transient events, the P_{GOOD} has a 25 µs blanking time.

Power Up Procedure

Before turning on the reference board, the user needs to finish jumper setup or use the default one (see section on mode selection). It is required to disable the SiC931 before making any changes to the jumpers.

Snubber Circuit

Snubber may be used when the user desires to decrease the peak voltage of switching node SW during turn on of the

high side switch. There are place holders on the reference board, R18, and C10, for the snubber.

PCB LAYOUT

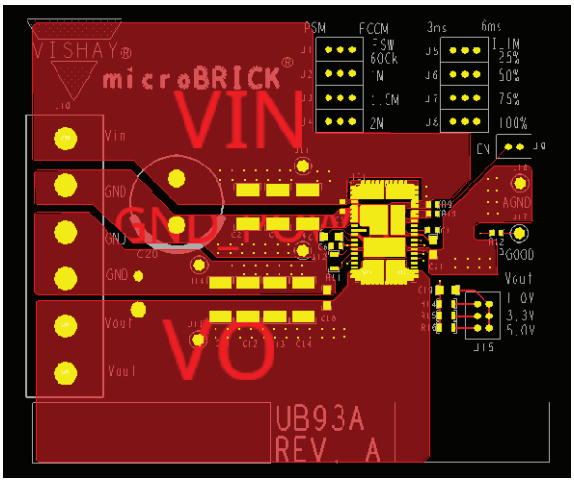


Fig. 3 - Top Layer

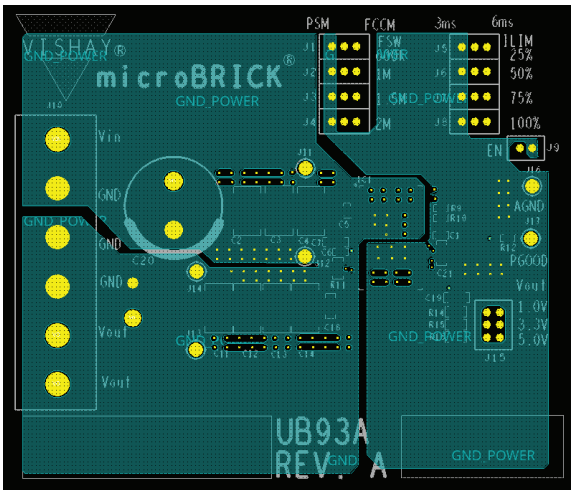


Fig. 6 - Inner Layer 2

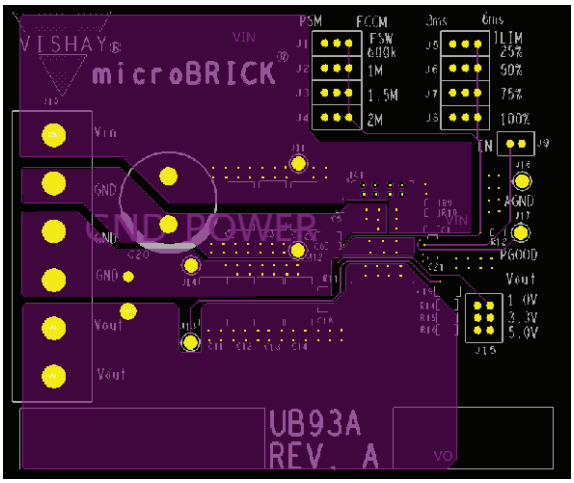


Fig. 4 - Inner Layer 3

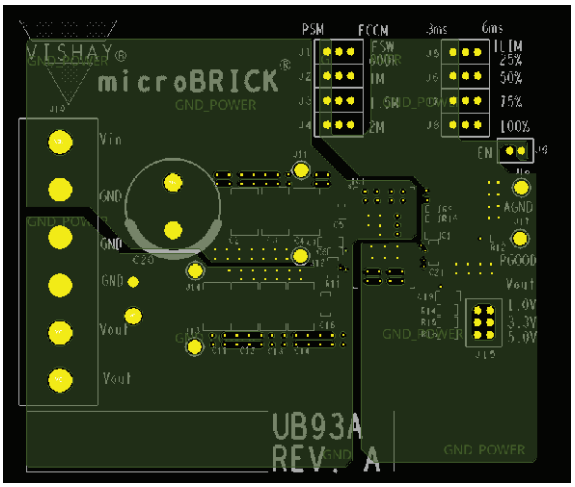


Fig. 7 - Inner Layer 4

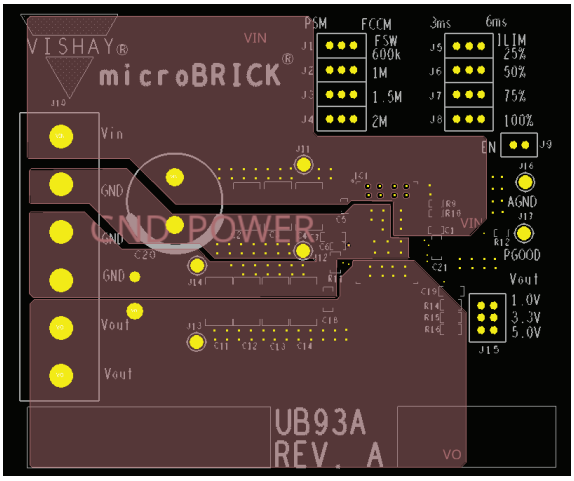


Fig. 5 - Inner Layer 5

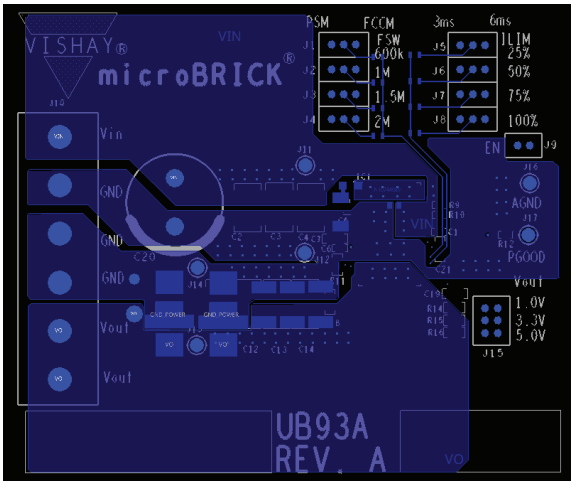
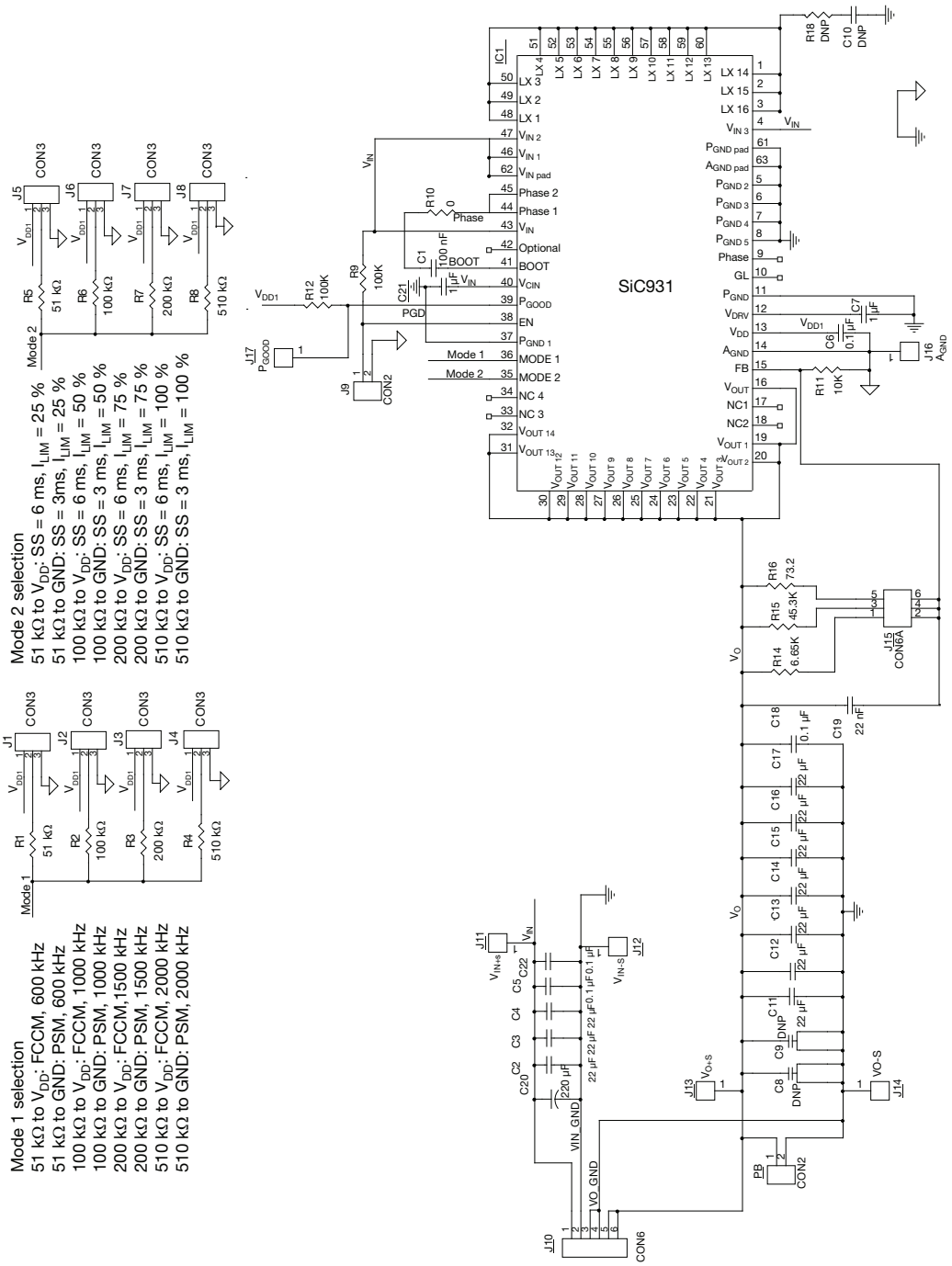


Fig. 8 - Bottom Layer

SCHEMATIC



SCHEMATIC, DESIGN, BILL OF MATERIALS, AND GERBER FILES FOR PCB FABRICATION

These files are as follows and available for download at www.vishay.com/power-ics/integrated-microbrick/list/product-79602/tab/documents/

- "*.DSN" for schematic design file
- "*.DBK" for data backup file for Orcad
- ".opj" Orcad project file. Any schematic work should always be opened with the opj file. Use of a DSN file for this purpose is not advised
- "*.xlsx" is the bill of materials (BOM) derived from the schematic
- "*.PDF" is the PDF version of the schematic from the "*.DSN" file

BILL OF MATERIAL REPORT

SYM_NAME	COMP_DEVICE_TYPE	COMP VALUE	DIGIKEY PN	SPEC FOR ORDER	QTY	REFDES
C0402-TDK1	CAPACITOR NON-POL_C0402-TDK1_10	0.1 µF	445-173610-1-ND	Cap. cer 0.1 µF, 50 V, X7R, 0402	4	C1, C5, C6, C22
C1210-TDK	CAPACITOR NON-POL_C1210-TDK_22U	22 µF	1276-3393-1-ND	Cap. cer 22 µF, 25 V, X7R, 1210	10	C2, C3, C4, C11, C12, C13, C14, C15, C16, C17
C0603-TDK1	CAP NP_C0603-TDK1_1U	1 µF	490-14409-1-ND	Cap. cer 1 µF, 25 V, X7R, 0603	2	C7, C21
POSCAP	POSCAP_POSCAP_DNP	DNP			0	C8
POSCAP	POSCAP_POSCAP_DNP	DNP			0	C9
C0603-TDK1	CAP NP_C0603-TDK1_DNP	DNP			0	C10
C0603-TDK1	CAPACITOR NON-POL_C0603-TDK1_0.	0.1 µF	445-8129-1-ND	Cap. ceramic 0.1 µF, 25 V, X7R, 0603	1	C18
C0603-TDK1	CAPACITOR NON-POL_C0603-TDK1_22	DNP			0	C19
CAP10P2X5	CAP_CAP10P2X5_220UF	220 µF	493-1319-ND	Cap. alu 220 µF, 20 %, 35 V, radial	1	C20
SIC931A	SIC931_SIC931A_SIC931	SiC931			1	IC1
MINIJUMPER3	CON3_MINIJUMPER3_CON3	CON3	M50-3530342		8	J1, J2, J3, J4, J5, J6, J7, J8
MINIJUMPER2	CON2_MINIJUMPER2_CON2	CON2	M50-3530242		1	J9
CON6	CON6_CON6_CON6	CON6	277-1581-ND		1	J10
TP30	CON1_TP30_VIN+S	V_{IN+S}	36-5000-ND	PC test point, red	2	J11, J13
TP30	CON1_TP30_VIN-S	V_{IN-S}	36-5001-ND	PC test point, black	3	J12, J14, J16
CON2x3	CONN HEADER VERT 6POS 1.27 mm	CON6A	S9015E-03-ND		1	J15
TP30	CON1_TP30_PGOOD	P_{GOOD}	36-5002-ND	PC test point, white	1	J17
2PROBE	CON2_2PROBE_CON2	CON2			1	PB
R0402-VISHAY1	R_R0402-VISHAY1_51K	51 kΩ		Res. SMD 51 kΩ, 1 %, 1/16 W, 0402	2	R1, R5
R0402-VISHAY1	R_R0402-VISHAY1_100K	100 kΩ		Res. SMD 100 kΩ, 1 %, 1/16 W, 0402	4	R2, R6, R9, R12
R0402-VISHAY1	R_R0402-VISHAY1_200K	200 kΩ		Res. SMD 200 kΩ, 1 %, 1/16 W, 0402	2	R3, R7
R0402-VISHAY1	R_R0402-VISHAY1_510K	510 kΩ		Res. SMD 510 kΩ 1 %, 1/16 W, 0402	2	R4, R8
R0402-VISHAY1	R_R0402-VISHAY1_0	0 Ω		Res. SMD 0 Ω JUMPER, 1/16 W, 0402	1	R10
R0603-VISHAY	RESISTOR_R0603-VISHAY_10K	10 kΩ		Res. 10 kΩ, 0.1 %, 1/8 W, 0603	1	R11
R0603-VISHAY	R_R0603-VISHAY_6.65K	6.65 kΩ, 0.1 %		Res. 6.65 kΩ, 0.1 %, 1/8 W, 0603	1	R14
R0603-VISHAY	R_R0603-VISHAY_45.3K	45.3 kΩ, 0.1 %		Res. 45.3 kΩ, 0.1 % 1/8 W 0603	1	R15
R0603-VISHAY	R_R0603-VISHAY_73.2	73.2 Ω, 0.1 %		Res. 73.2 Ω, 0.1 %, 1/8 W, 0603	1	R16
R1206-VISHAY	RESISTOR_R1206-VISHAY_DNP	DNP			0	R18
				UB93A	1	PCB
			NPB02SVFN-RC	JUMPER, 1.27 mm, gold	3	