# P-Channel 60 V (D-S) MOSFET

DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC
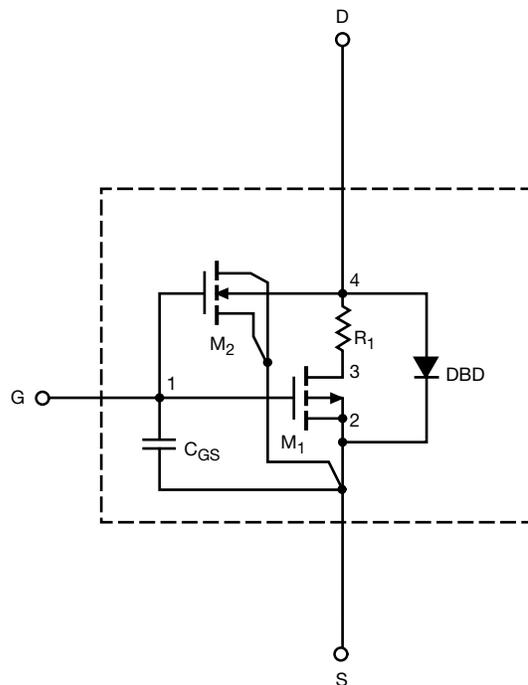
Note
- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

For technical questions, contact: pmostechsupport@vishay.com

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	2.8	-	V
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = -10 V, V_{GS} = -10 V	2.2	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -500 mA	3	3.1	Ω
		V_{GS} = -4.5 V, I_D = -25 mA	4.4	5.5	
Forward Transconductance [a]	g_{fs}	V_{DS} = -10 V, I_D = -500 mA	170	180	S
Diode Forward Voltage [a]	V_{SD}	I_S = -200 mA, V_{GS} = 0 V	-0.75	-0.90	V
Dynamic [b]					
Total Gate Charge	Q_g		0.50	-	nC
Gate-Source Charge	Q_{gs}	V_{DS} = -30 V, V_{GS} = -10 V, I_D = -500 mA	0.12	0.12	
Gate-Drain Charge	Q_{gd}		0.14	0.14	

Notes

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)
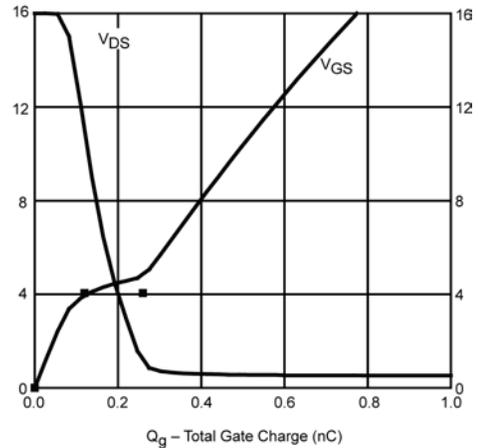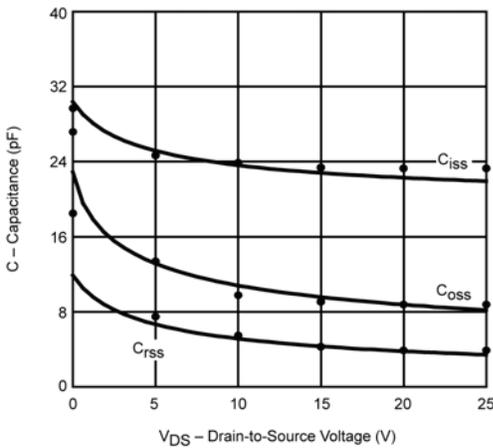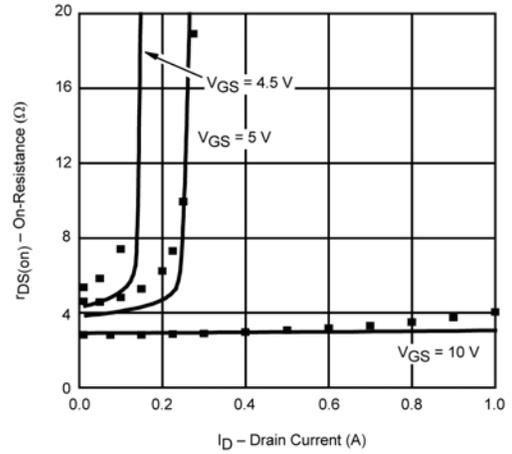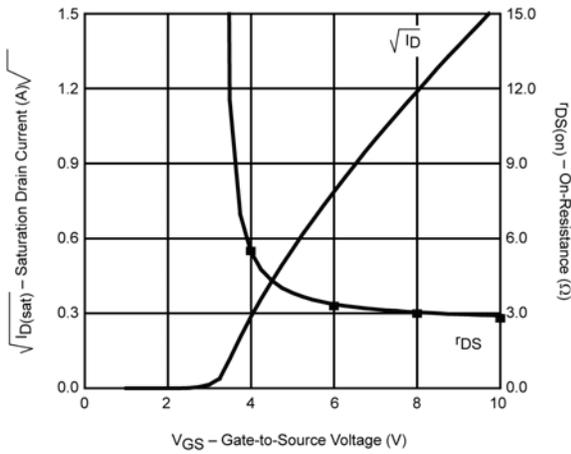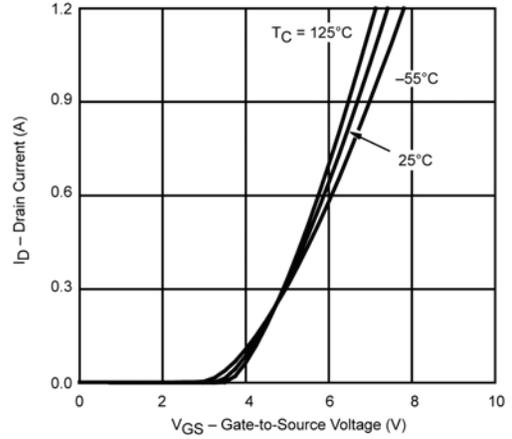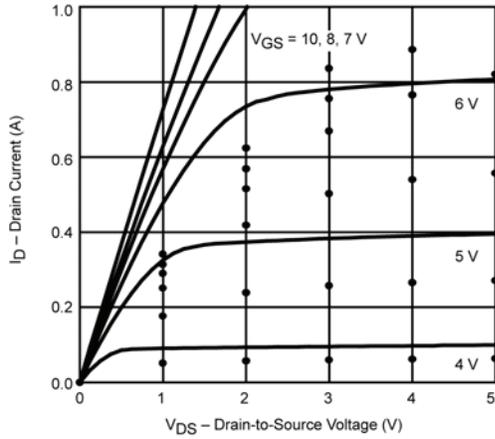
Note
- Dots and squares represent measured data.

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