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**Vishay Siliconix** 



PRODUCT SUMMARY						
V <sub>DS</sub> (V)	40					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = 10 V	0.00099					
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = 4.5 V	0.00136					
Q <sub>g</sub> typ. (nC)	182					
I <sub>D</sub> (A) <sup>d</sup>	200					
Configuration	Single					

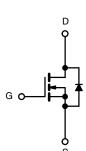
# N-Channel 40 V (D-S) MOSFET

### FEATURES

- TrenchFET<sup>®</sup> Gen IV power MOSFET
- Maximum 175 °C junction temperature
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

#### APPLICATIONS

- Power supply
  Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management
- OR-ing



RoHS COMPLIANT

HALOGEN

FREE

N-Channel MOSFET

ORDERING INFORMATION				
Package	D <sup>2</sup> PAK (TO-263-7L)			
Lead (Pb)-free and halogen-free	SUM40014M-GE3			

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \degree C$ , unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-source voltage	V <sub>DS</sub>	40	V			
Gate-source voltage	V <sub>GS</sub>	± 20	V			
Continuous ducin ourrent (T 150 °C)	T <sub>C</sub> = 25 °C		200 <sup>d</sup>			
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 70 °C	– I <sub>D</sub> –	200 <sup>d</sup>			
Pulsed drain current (t = 100 µs)	I <sub>DM</sub>	400	A			
Avalanche current		I <sub>AS</sub>	70			
Single avalanche energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	245	mJ		
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	P	375 <sup>b</sup>	w		
	T <sub>C</sub> = 125 °C	- P <sub>D</sub> -	125 <sup>b</sup>	VV		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-ambient (PCB mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-case (drain)	R <sub>thJC</sub>	0.4	0/10	

#### Notes

a. Duty cycle  $\leq$  1 %

b. See SOA curve for voltage derating

c. When mounted on 1" square PCB (FR4 material)

d. Package limited

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### SUM40014M

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•		. <u> </u>		
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 10 mA$	40	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.1	-	2.4		
Gate-body leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 250	nA	
		$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μA	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	150		
		$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	5	mA	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \geq 10~V,~V_{GS} = 10~V$	100	-	-	А	
	D	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	-	0.00082	0.00099	Ω	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	-	0.00113	0.00136		
Forward transconductance <sup>a</sup>	<b>g</b> fs	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	-	140	-	S	
Dynamic <sup>b</sup>				•			
Input capacitance	C <sub>iss</sub>		-	15 780	-	pF	
Output capacitance	Coss	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V, f = 1 MHz	-	2280	-		
Reverse transfer capacitance	C <sub>rss</sub>		-	90	-		
Total gate charge <sup>c</sup>	Qg		-	182	275	nC	
Gate-source charge c	Q <sub>gs</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	41	-		
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	9	-		
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.5	2.4	4.8	Ω	
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>		-	20	40		
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, \text{ R}_{L} = 5 \Omega$	-	10	20		
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_{D}\cong10\;A,V_{GEN}=10\;V,R_{g}=1\;\Omega$	-	100	200	ns	
Fall time <sup>c</sup>	t <sub>f</sub>		-	35	70		
Drain-Source Body Diode Ratings a	nd Characteris	stics <sup>b</sup> (T <sub>C</sub> = 25 °C)					
Pulsed current (t = 100 µs)	I <sub>SM</sub>		-	-	600	А	
Forward voltage <sup>a</sup>	V <sub>SD</sub>	$I_{F} = 10 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.72	1.5	V	
Reverse recovery time	t <sub>rr</sub>		-	55	80	ns	
Peak reverse recovery charge	I <sub>RM(REC)</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs	-	2.2	5	А	
Reverse recovery charge	Q <sub>rr</sub>		-	0.065	0.13	μC	

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing

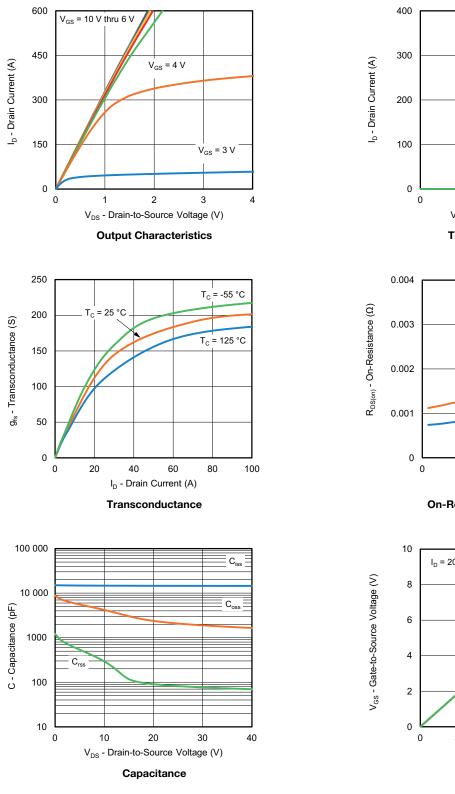
c. Independent of operating temperature

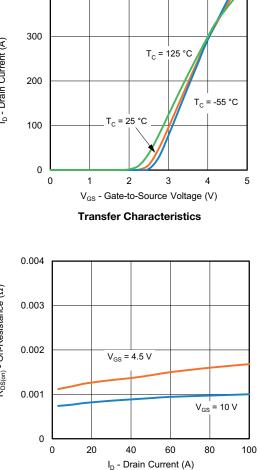
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



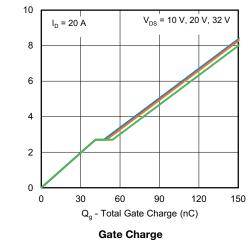
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### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)





**On-Resistance vs. Drain Current** 



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3

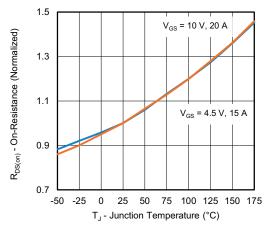
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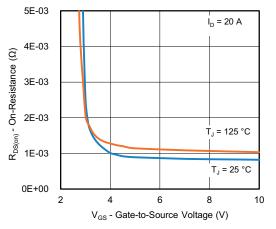


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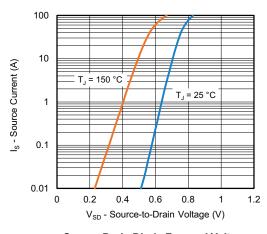
### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



**On-Resistance vs. Junction Temperature** 



**On-Resistance vs. Gate-to-Source Voltage** 



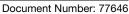
Source Drain Diode Forward Voltage

Note

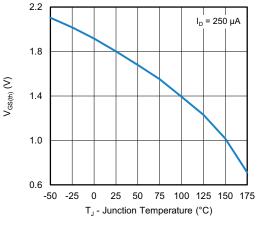
a.  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

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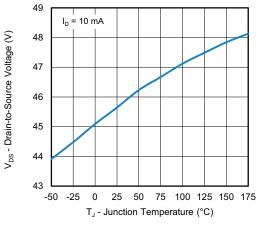
4



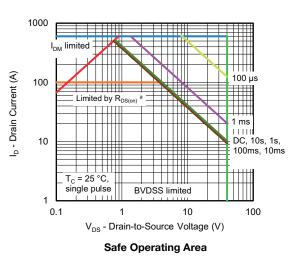
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**Threshold Voltage** 



Drain Source Breakdown vs. Junction Temperature

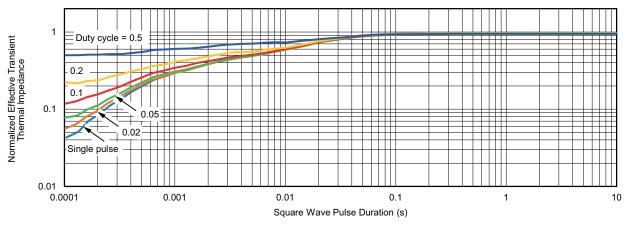




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### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

• The characteristics shown in the two graphs

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- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

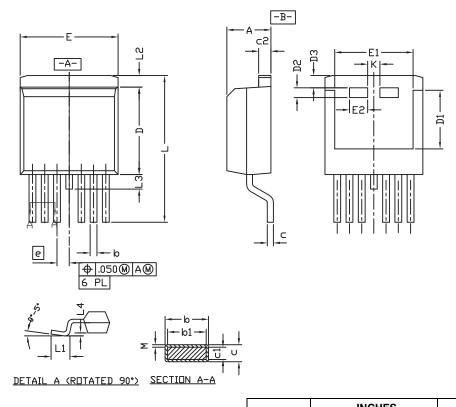
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?77646</u>.



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## D<sup>2</sup>PAK (TO-263-7L) Case Outline



#### Notes

- 1. Plane B includes maximum features of heat sink tab and plastic
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils
- 3. Pin to pin coplanarity max. 4 mils
- 4. Lead thickness 25 mils
- 5. For SUM part numbers lead thickness is 24 mils to 29 mils
- 6. For reference only
- 7. Use inches as the primary measurement
- 8. This feature is only for SUM

	INCHES		MILLIN	IETERS	
DIM.	MIN.	MAX.	MIN.	MAX.	
А	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
c* SUB	0.012	0.018	0.305	0.457	
c* SUM	0.022	0.028	0.559	0.711	
c1	0.018	0.025	0.457	0.635	
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.260	0.280	6.604	7.112	
D2	0.046	0.050	1.168	1.270	
D3	0.045	0.055	1.143	1.397	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.072	0.078	1.829	1.981	
е	0.050 BSC		1.27	BSC	
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010	BSC	0.254	0.254 BSC	
М	-	0.002	-	0.050	
ECN: T22-0410-Rev. D, 19-Sep-2022 DWG: 6006					

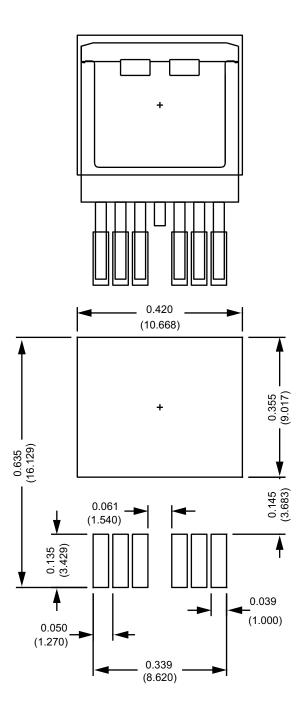
Document Number: 63782





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## Recommended Land Pattern D<sup>2</sup>PAK (TO-263-7L)



Revision: 23-Jul-2020



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